Evolvable Hardware for Sensors

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Task Lead:

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Group

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Evolvable Hardware for Sensors

Task Lead: A. Stoica, JPL

Goal

Demonstrate new evolution capabilities in space electronics, in particular in space sensing systems.

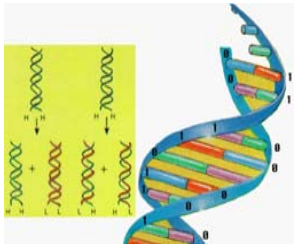
Near Term Objectives

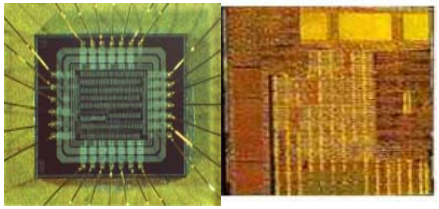
Demonstrate on-chip evolution on custom-made, evolution-oriented field programmable transistor arrays.

- Demonstrate EHW for versatility/optimal operation
  - Adaptation of sensor systems
- Demonstrate EHW for survivability
  - Fault-tolerance and self-healing

Key Innovation

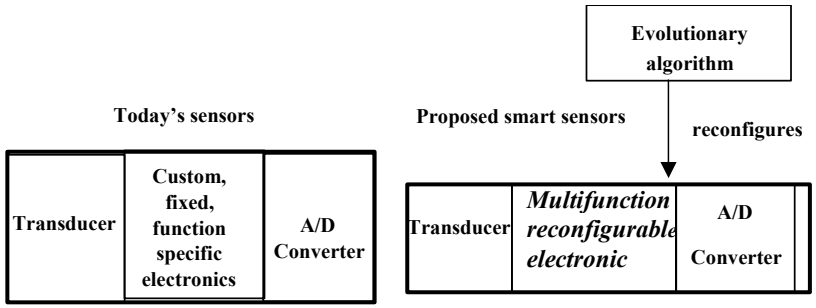
Combine flexibility of reconfigurable/tunable hardware with reconfigguration/search power of evolutionary algorithms in space sensing systems





Reconfigurable Sensing deivice

Evolutionary Processor running SW-GA



NASA Relevance

Provide space sensing systems with

- versatility, survivability for long duration missions, achieving optimal operation in harsh, unknown environments.
- maintaining functionality, coping with faults and changing environments

Accomplishments to date

- **Develop and demonstrate a flexible evolvable hardware testbed**
- **On-chip evolution of 4-bit digital-to-analog (D/A) and 3-bit analog-to-digital (A/D) converters**
- **On-Chip evolution of high/low band pass filters, tunable frequency filter**

Schedule

- FY'02: Develop on-chip evolution on custom-made evolution-oriented FPTA for sensor processing and basic fault-tolerant experiments.
- FY'03: Evolution for survivability in radiation and extreme temperature environments.
- FY'04: Develop a new dieHard architecture integrating the reconfigurable area, sensing area and evolution mechanisms

Team Members/Facilities/Collaborators

- JPL Personnel:
  - A.Stoica, Ph.D. Task Manager, over-see all the activities and coordinate technical performance.
  - D.Keymeulen, Ph.D: develops the required evolution S/W and sensor interface.
  - R. Zebulum, Ph.D: prepares necessary H/W and perform experiments
  - V. Duong, Msc: prepares necessary H/W and perform experiments
  - M. Ferguson, Msc: interfaces with S/W and H/W and assist in the evolution experiments
  - T. Daud, Ph.D.: management support: help with financial and programmatic management and preparation of SBAR. He also helps in line management related issues and subcontract management
- Facilities:
  - **Evolvable Hardware Testbed –** allows to implement Genetic Algorithms on a stand-alone digital signal processor (DSP) controlling the evolution-oriented hardware device.
  - **Extreme Environment Testbed –** allows to investigate the impact of the Genetic Algorithms on the hardware evolution in extreme environment.
- Collaborators:
  - **Presently there is no partnering plan.**
  - **A participation with Portland University has been developed for this task:** Using Lattice ispPAC10 equipped testbed, PU is investigating particular GA features that contribute to high speed evolution. This will lead insight into evolution processing, never attempted so far.

Former Work/Leverage

- Evolution Oriented Device (FPTA-2)
  - **Former work:** we developed the first evolution-oriented programmable device with reconfigurability at transistor level. This enables, for the first time, directly in silicon (thus at high speeds) automated circuit synthesis using evolutionary algorithms.
  - **Leverage:** FPTA-2 allows interfacing directly with sensors and performing evolution on-chip, at speeds 3 to 6 orders of magnitude faster than in simulations.
- Stand-alone Board-level Evolvable System
  - **Former work:** A complete stand-alone board-level evolvable system was built by integrating the FPTA2 and a DSP implementing a collection of architecture-independent routines to perform tasks related to evolution in hardware.
  - **Leverage:** the platform allows performing adaptation of the sensor-processing array ensemble.
- Extreme Environment Testbed:
  - **Former work:** we build an extreme temperature testbed to achieve evolution on FPTA with die temperatures exceeding 250C while staying below 250 C on the package.
  - **Leverage:** the testbed allows dealing with hardware-specific effects (of both the processing array and sensors) related to faults and degradation that are induced by temperature.

Achieved and Planned Experiments for FY'02

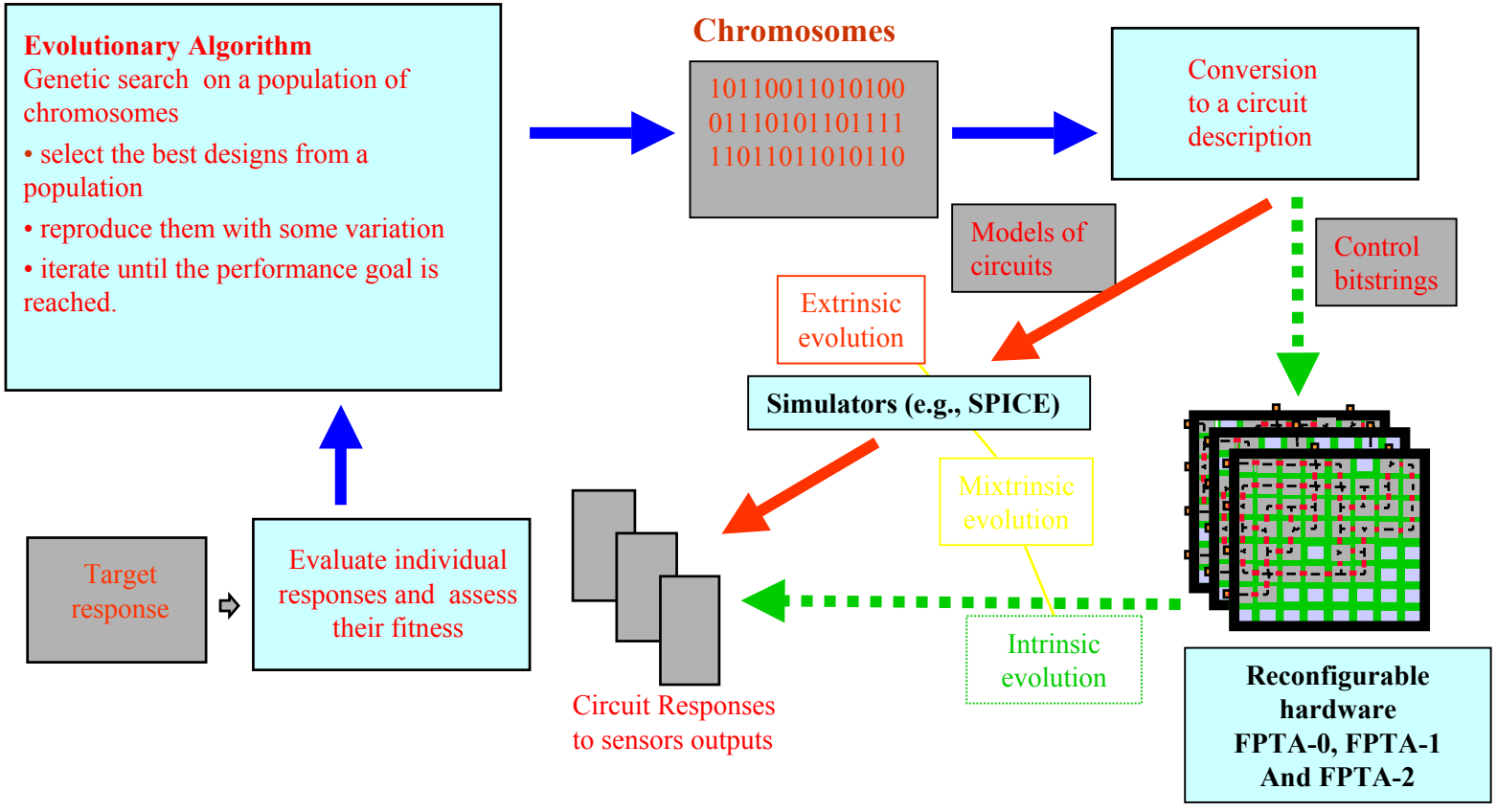
- ✓ On-chip evolution of computational circuits for sensor processing:
  - **Experiments demonstrated using the stand-alone board level evolvable system**
    - ✓ on-chip evolution of data converters
    - ✓ on-chip evolution of adaptive filters
  - **TRL level: 2**
  - **Risk:** Low (perform similar experiments in simulation)
- On-chip evolution of basic fault-tolerant experiments :
  - **Experiments will demonstrate using the stand-alone board level evolvable system**
    - a fault-recovery of circuits from up to 4 faults
  - **TRL level: 2**
  - **Risk:** Low (preliminary experiments were done with FPTA-0)

Outline of the talk

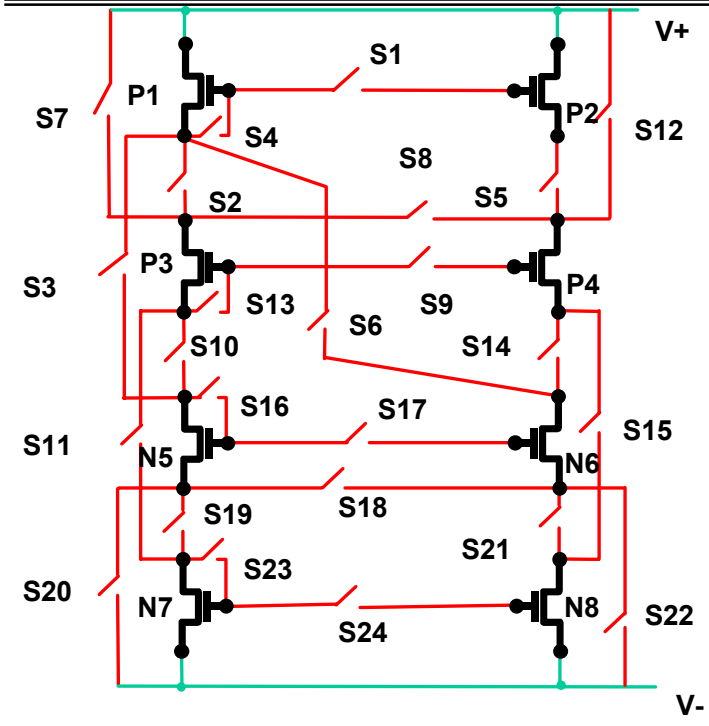
1. Evolvable Hardware Technology FPTA
   Field Programmable Transistor Array (PTA, FPTA1, FPTA2)
2. Evolvable Hardware Platform SABLES
   A stand-alone board-level evolvable system
3. Evolvable Hardware for Sensors
   - Evolvable Sensing
   - Data Converters (D/A – A/D)
   - Adaptive filter (Low/High/Tunable) – AGC/Oscillator
   - Graphical Interface
4. Future Efforts and Challenges

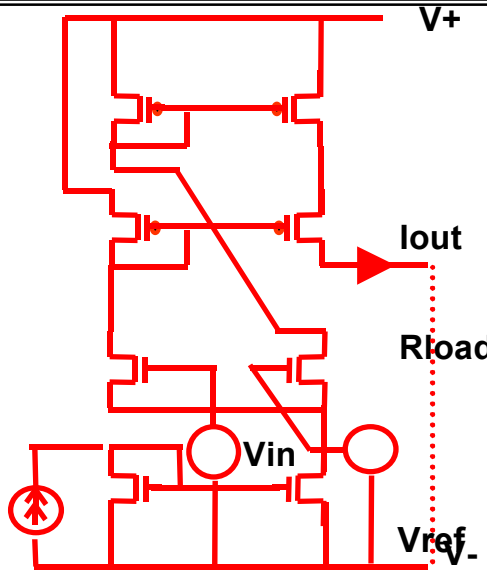
Evolvable Hardware in Electronics

Evolutionary synthesis and adaptation of electronics circuits

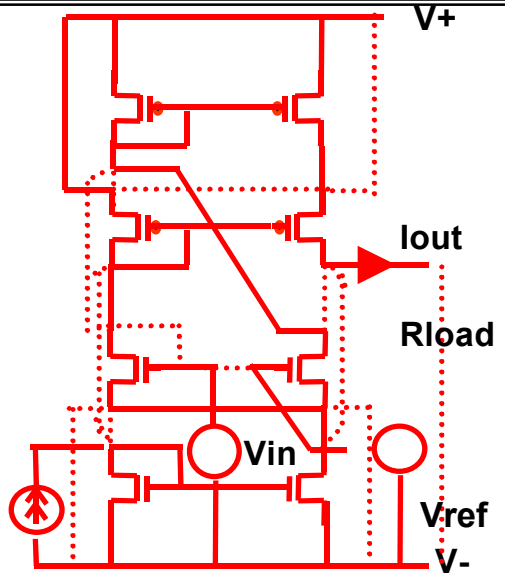


Programmable Transistor Array Cell – FPTA0



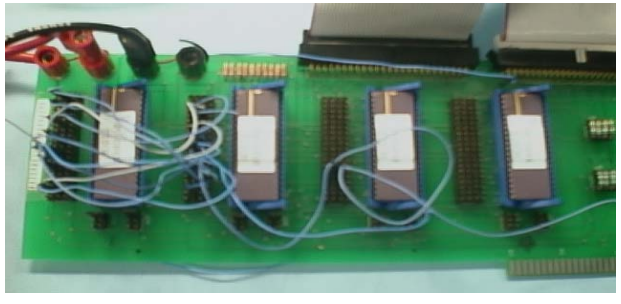


Human Design

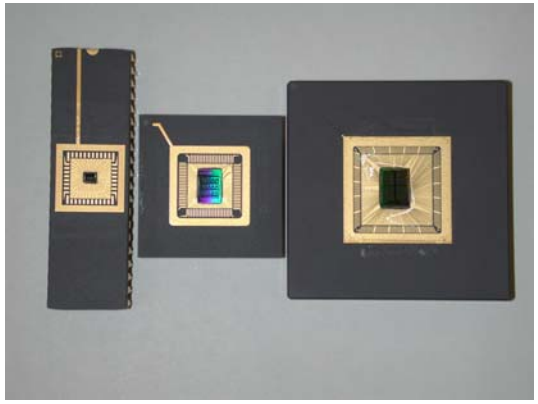


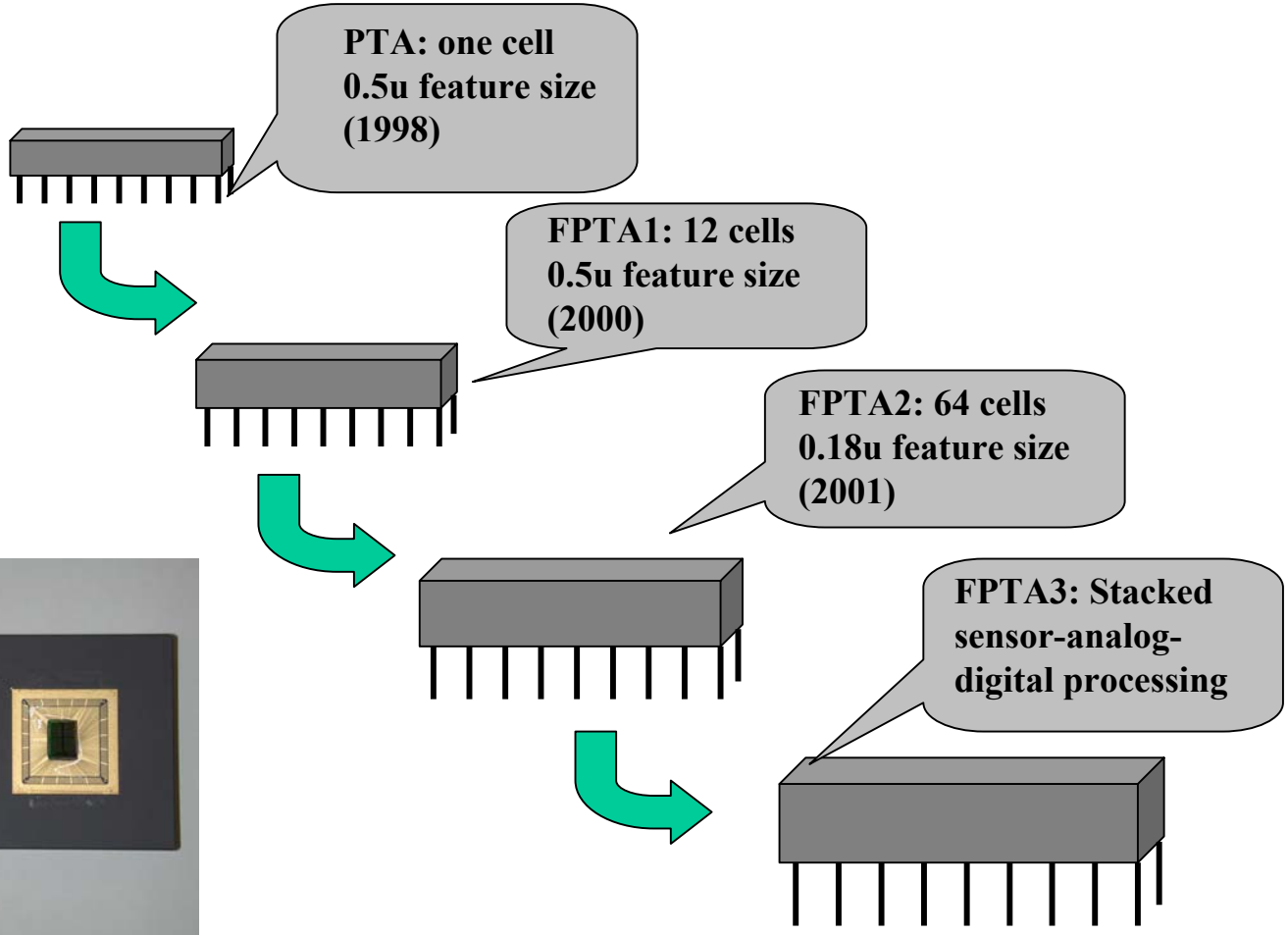
Leakage through finite resistance OFF

- 24 programmable switches: sufficient number for meaningful topologies
- Chromosomes give the value ON-OFF of the switches
- All the terminals are connected via switches to expansion terminals
- CMOS (0.5 μ) - MOSIS



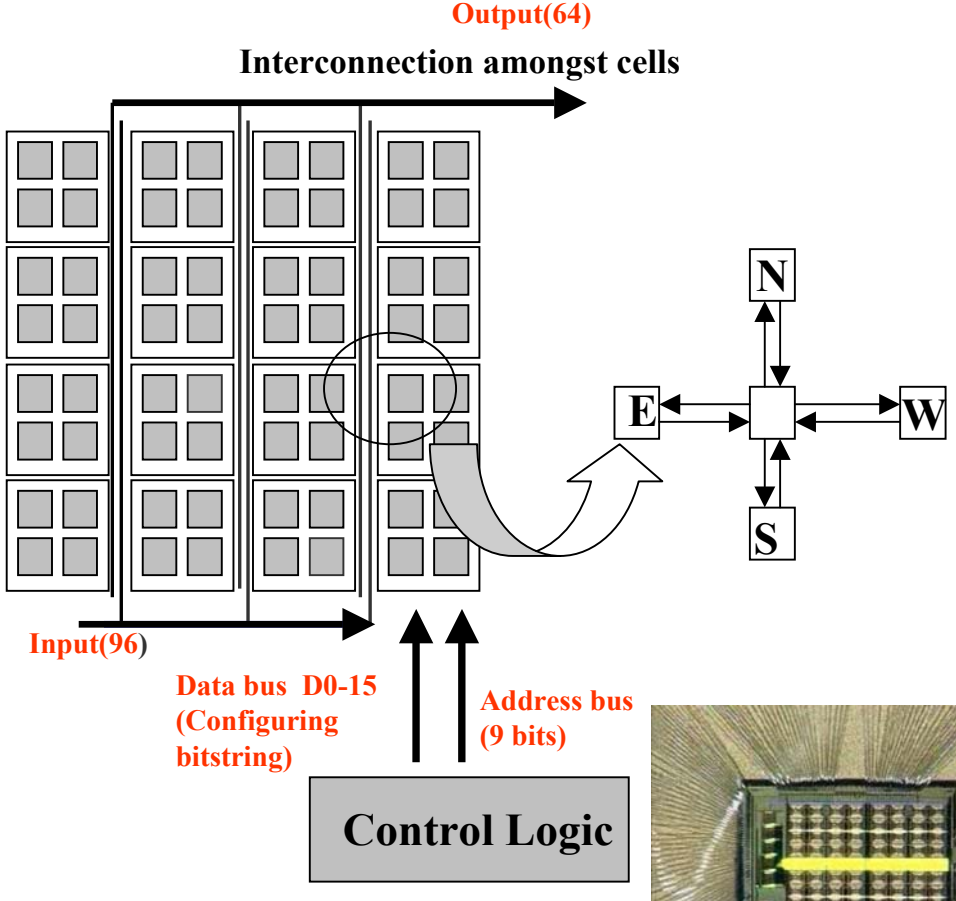
Evolvable Hardware with the FPTA Series



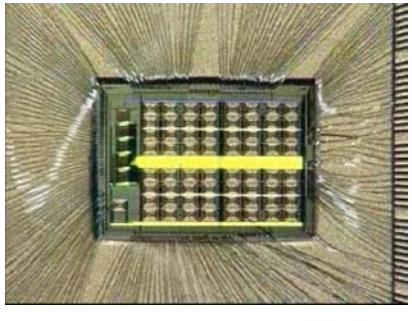


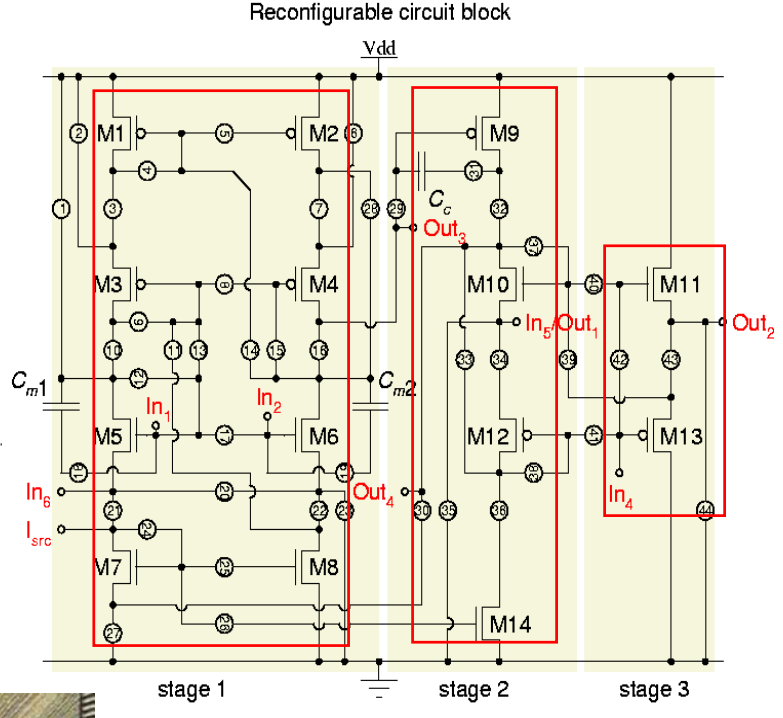
Programmable Transistor Array Cell – FPTA2

- Implementation of an evolution-oriented reconfigurable architecture (EORA)



Chip Architecture





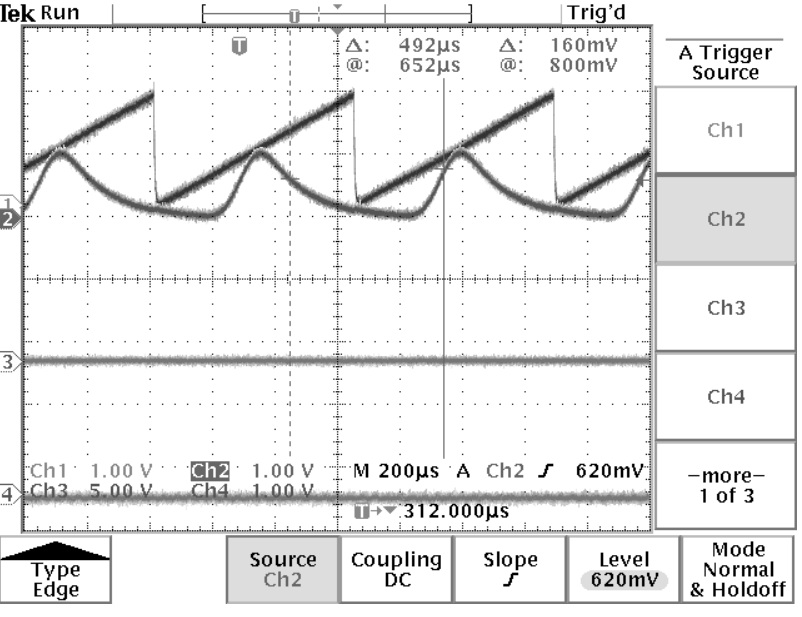
Cell Schematic

FPTA-2 Features

- **Basic features**
  - **Technology: TSMC 0.18u, V_{dd}=2 Volt**
  - **Area 5mm x 7mm;**
  - **64 cells;**
  - **Total of 256 pins;**
  - **96 analog/digital inputs and provide 64 analog/digital outputs;**
  - **16 bits data bus/9 bits address bus control logic;**
  - **About 5000 programming bits;**

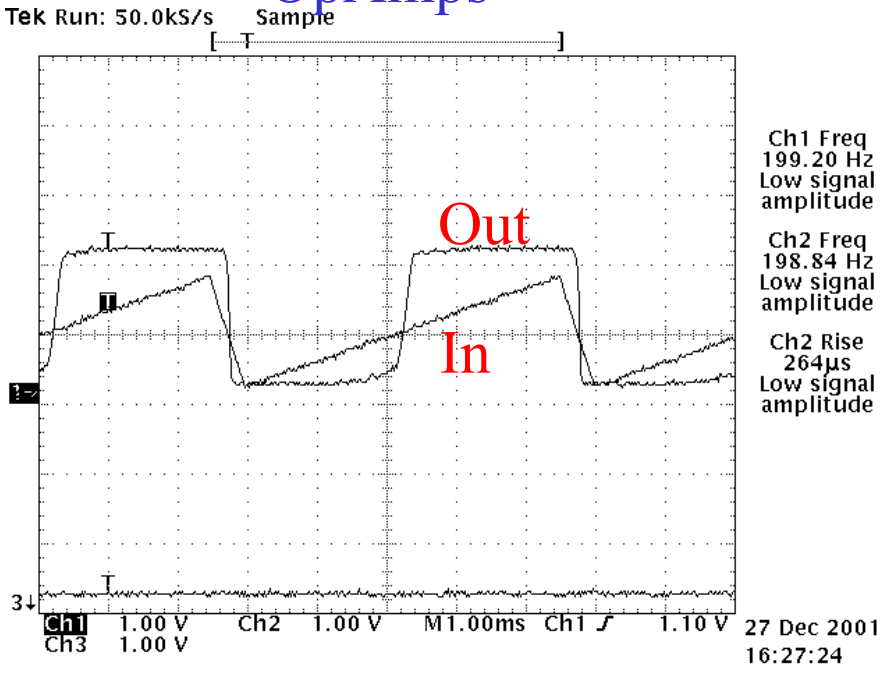
FPTA2 - Tested Circuits

Gaussian



- FPTA: cell 1
- Inputs:
  - In1, In2
  - ramp 0 to 2 Volt
  - Frequency: 3 KHz
- Output: Out3

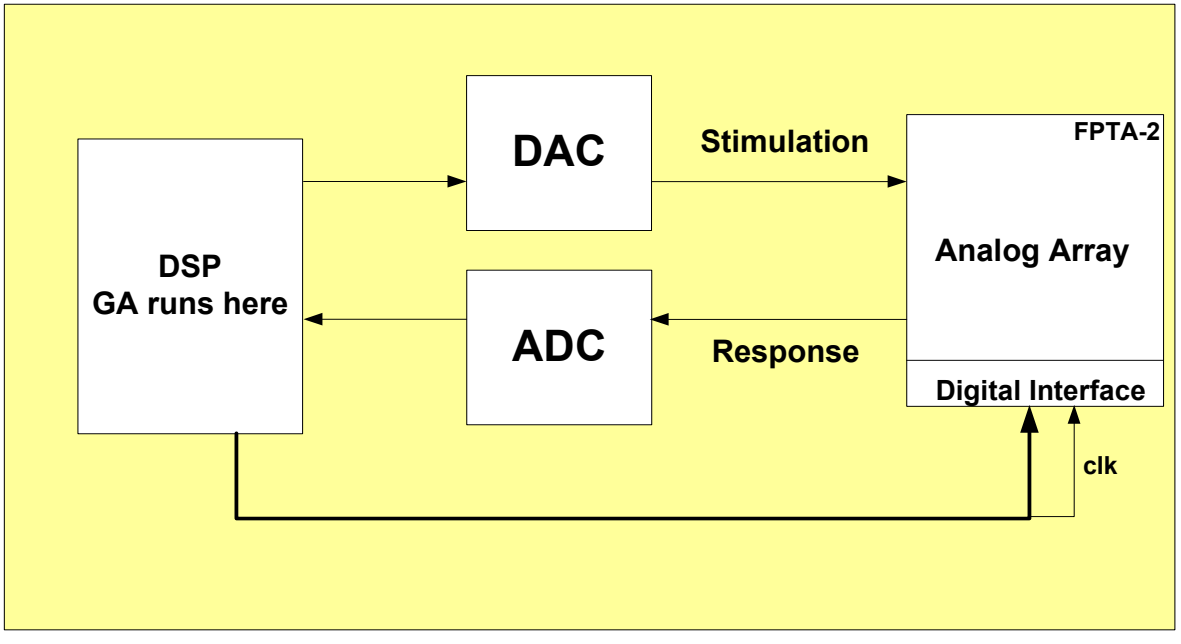
OpAmps

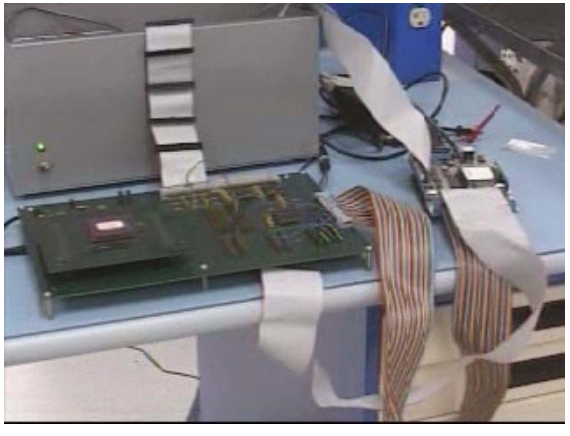


- FPTA: cell 1
- Inputs:
  - differential inputs
  - In1(In) and In2(0.9Volt)
  - Frequency: 200Hz (up to 100KHz)
- Output: Out2

Evolvable Hardware Platform (SABLE)

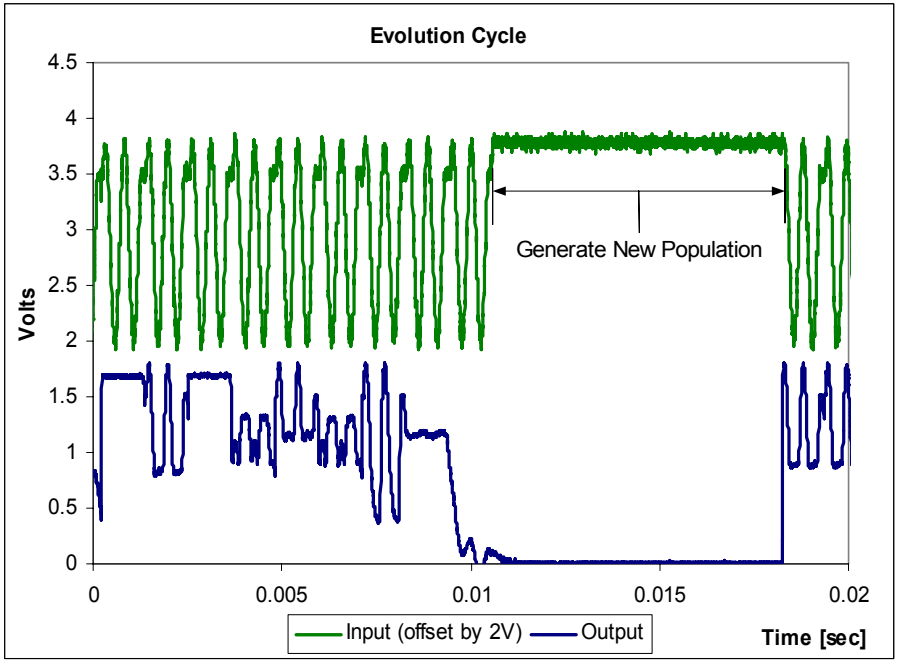
A Stand-Alone Board-Level Evolvable System

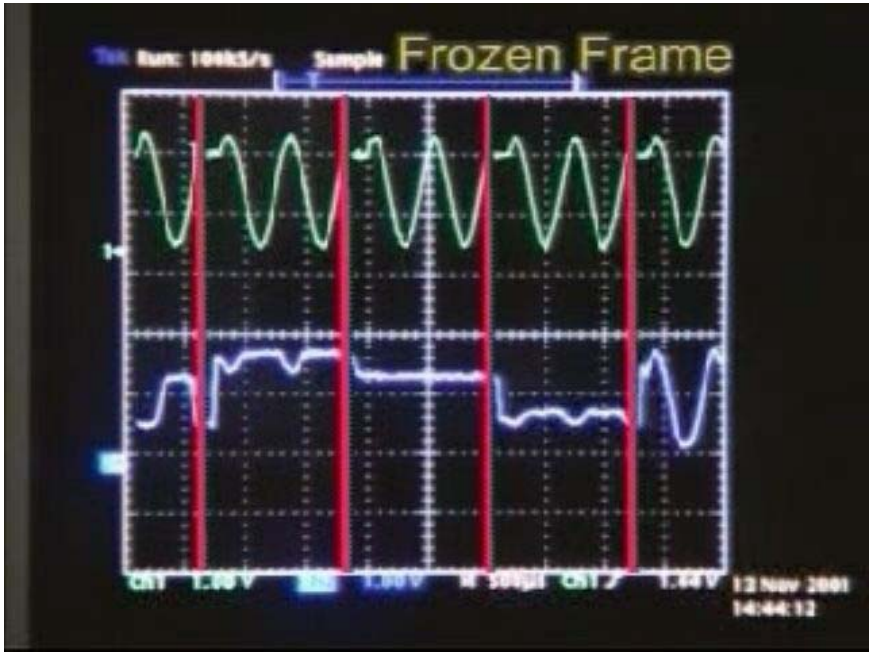




- FPTA – fast evaluation compared to simulation of SPICE netlist
- DSP + FPTA
  - Fast download for evaluation of individuals
  - Good architecture for moving to a self-reconfigurable system-on-a-chip
    - Fault-tolerant solution on a chip
    - Sensors, actuators

Evolution with SABLE

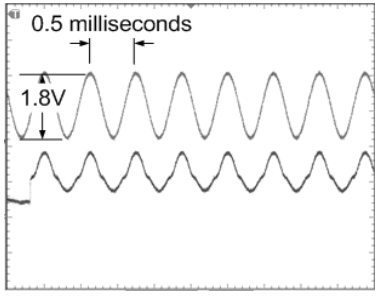




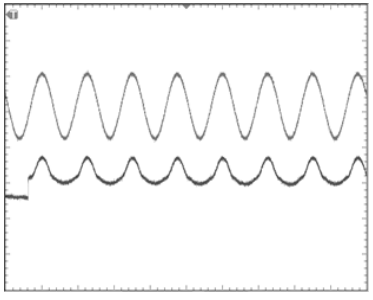
- Evolution of a Half-wave rectifier circuit: Excitation input of 2kHz sine wave of amplitude 2V
  - 9% elite percentage, 70% crossover, 4% mutation; 100 individuals population;
  - 20 seconds experiments
- Stimulus-Response wave form during the evaluation of a population in one generation (left) and for 3 individuals in the population (right)

SABLE Performance

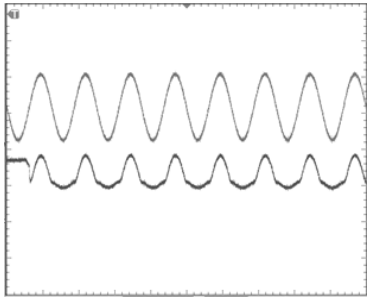
SABLES system: best individual through generation



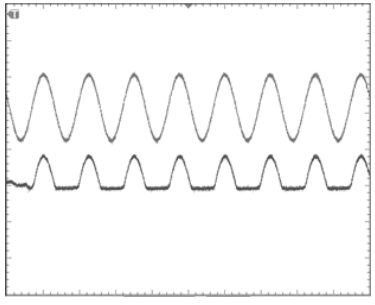
generation 1 (0.2 sec)



generation 5 (1 sec)

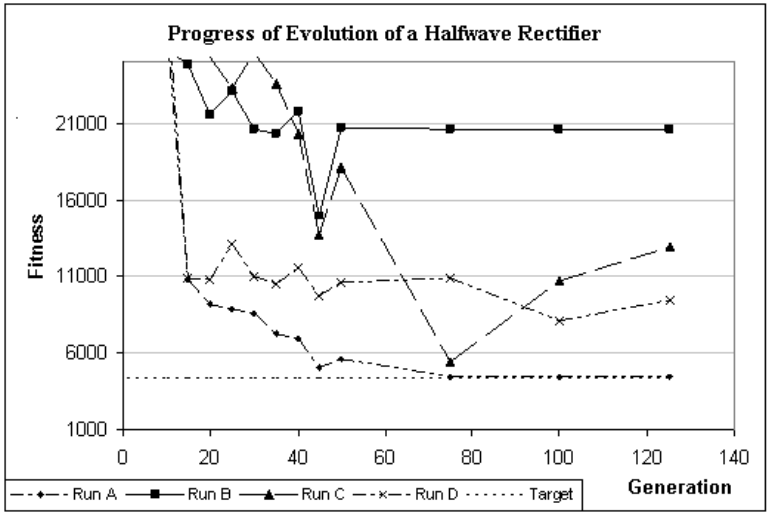


generation 50 (10 sec)

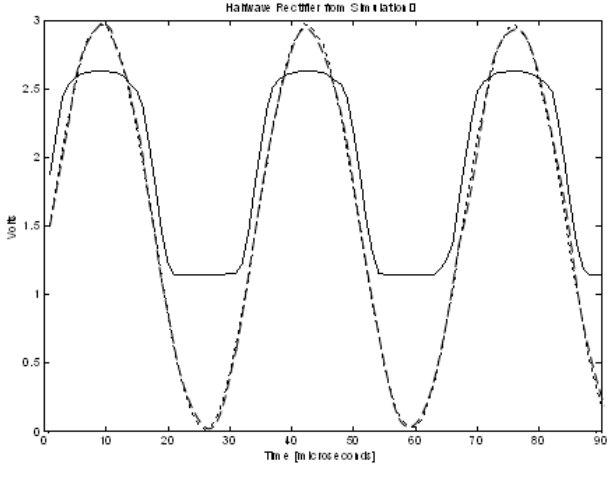


generation 82 (17 sec)

SABLES system: fitness function as generations progress



Super Computer system



After about 200 generations (40 min~2400 sec)

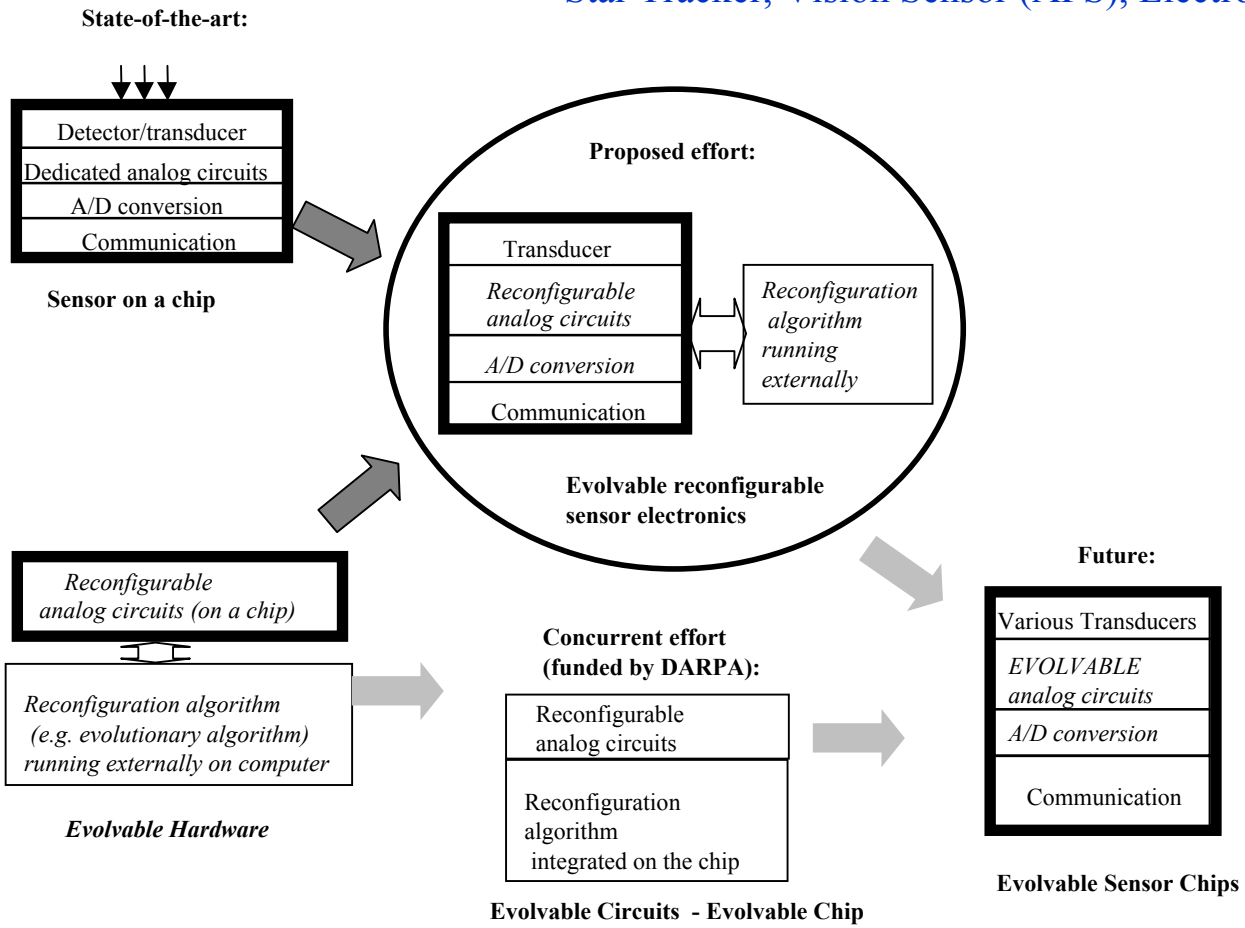
Movie of SABLES (DVD)

Evolvable sensing

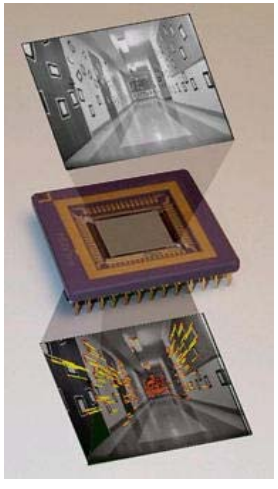
Smart sensing – evolve reconfigurable sensors

Replace/self-configure signal conditioning electronics in flight instruments.

Star Tracker, Vision Sensor (APS), Electrometer

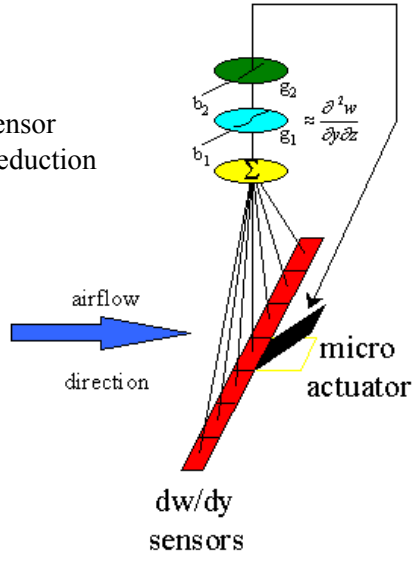


Evolvable Sensor Electronics

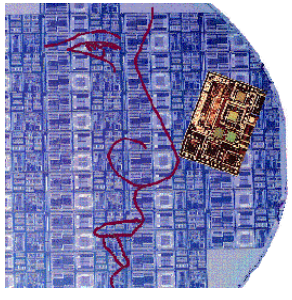


E-EYE
motion and
optical flow
visual guidance

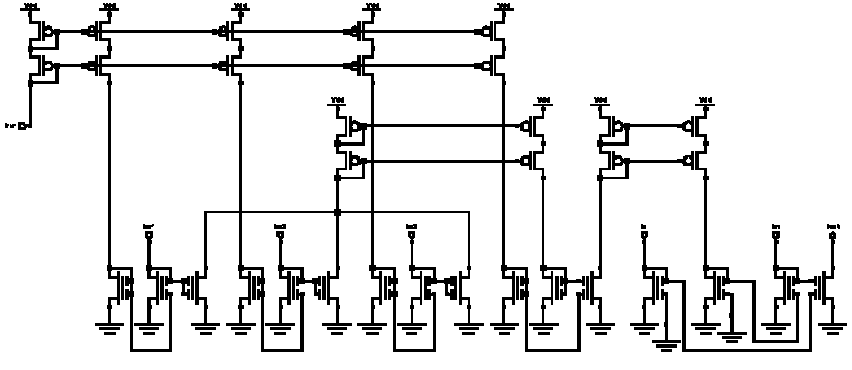
E-SKIN
Micro Surface
Shear Stress Sensor
Active Drag Reduction



E-NOSE
chemical sensors
sensitive to gas, etc
smell-guidance



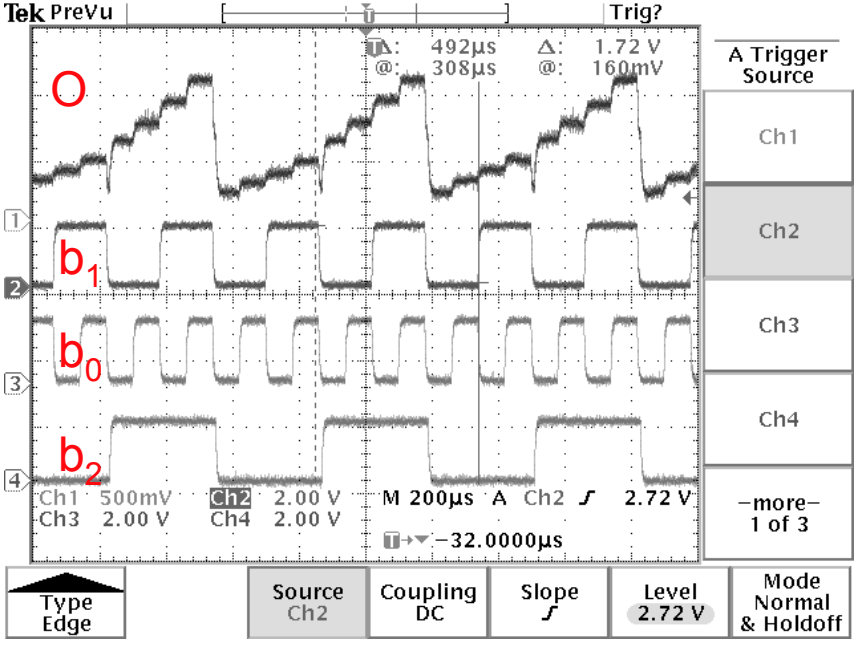
- Multipurpose
- Reconfigurable
- Adaptive
- Self-configurable

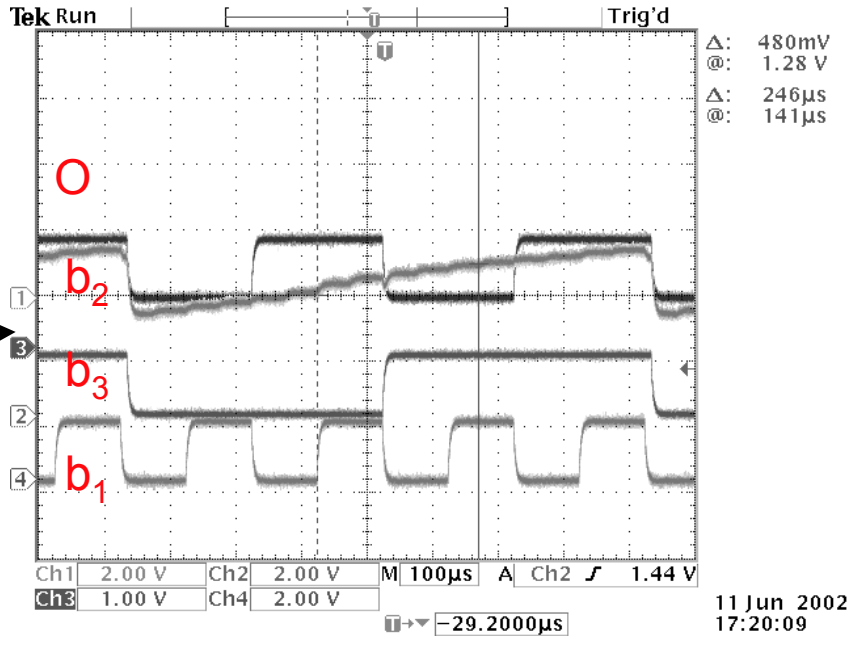


Evolution of Digital-to-Analog Converters (DACs)

- Reconfigurable Cell (FPTA-2)
  - 8 cells: 0,1,2,3,4,5,6,7.
  - Input: 4 Digital Inputs (0 to 2 Volt – 10 kHz)
- Evolution Mechanism:
  - Hierarchical Evolution: 4 bit DAC evolved from previously evolved 3 bit DAC (cells 0,1,2,3)
  - Fitness Function: Absolute error to the target;
- Genetic Algorithm
  - 400 individuals
  - Chromosome: 500 bits
  - less than 50 generations – 1 min

Evolution of Digital-to-Analog Converters (DACs)





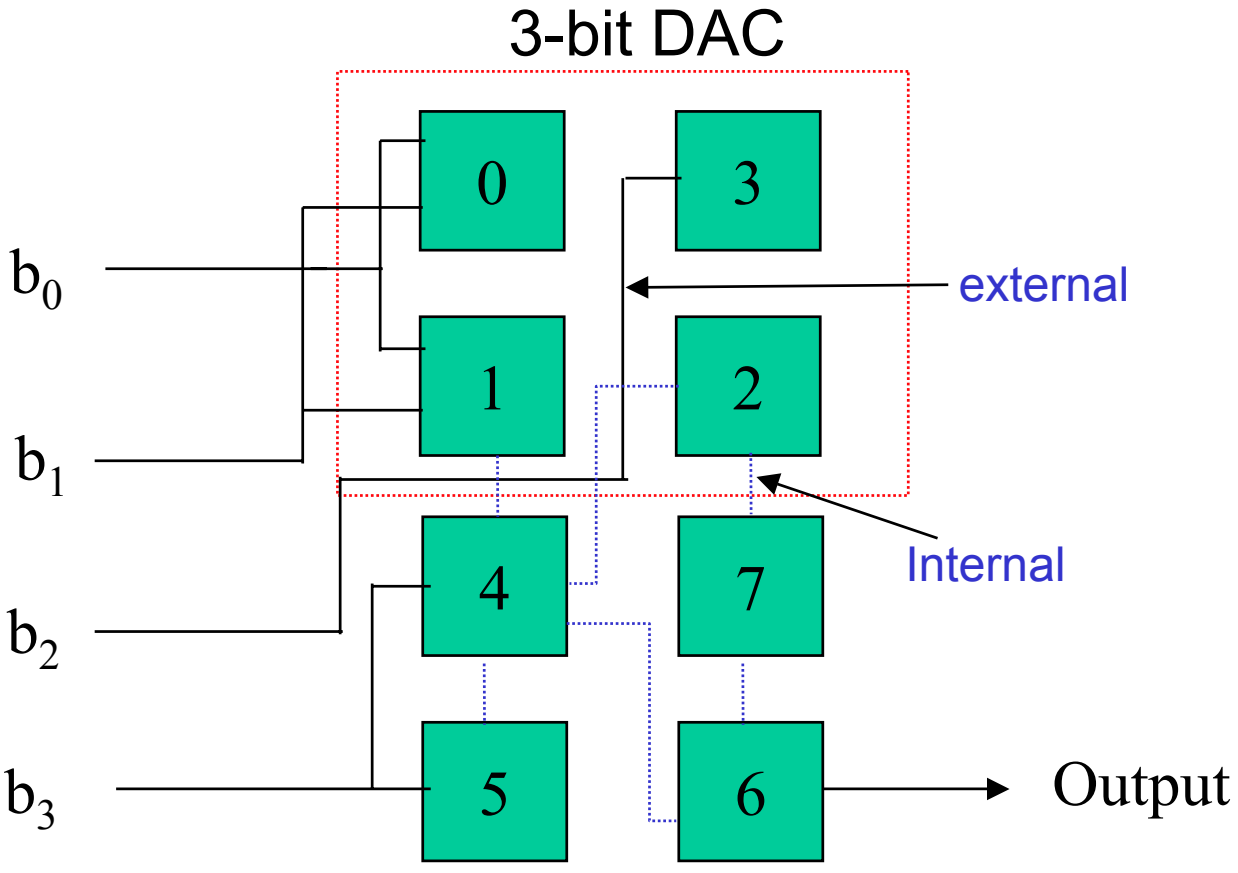
3 bit DAC:

- 4 Cells of FPTA-2
- Input 10 kHz
- LSB = 0.20 Volt
- Full-Scale V.: 0 to 1.41 V

4 bit DAC:

- 8 Cells (4 fixed to 3-bit DAC).
- Input 10 kHz
- LSB = 0.094 Volt
- Full-Scale Voltage: 0 to 1.41 Volt

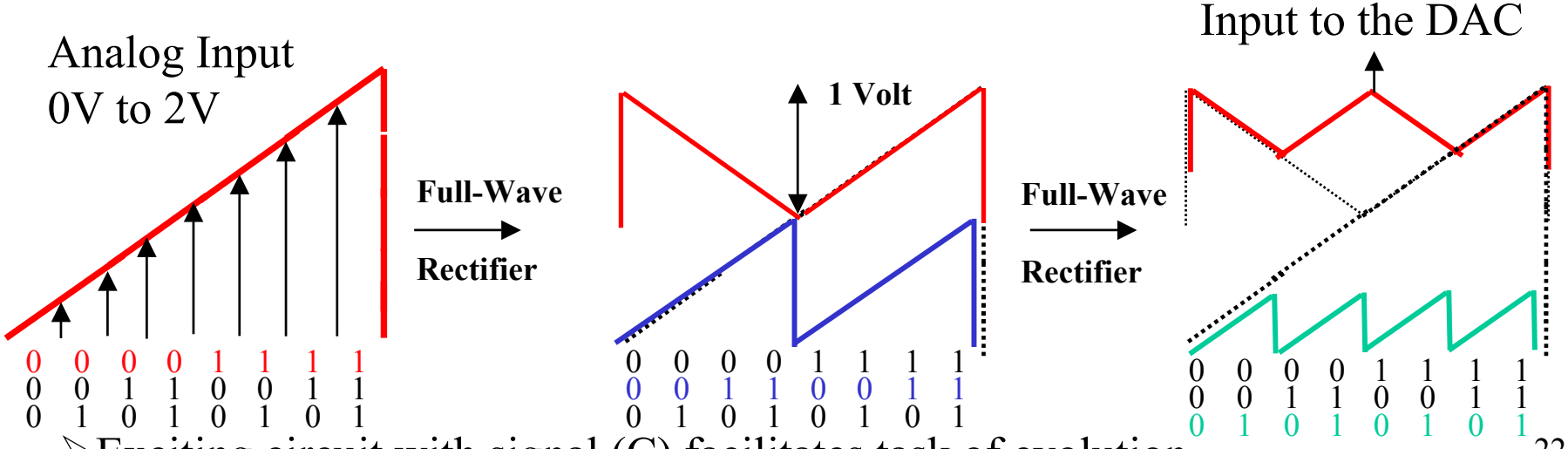
Circuit Schematic of evolved 4-bit DAC



b_0, b_1, b_2, b_3: Digital Inputs (b_0 – LSB, b_3-MSB)
O – Analog Output

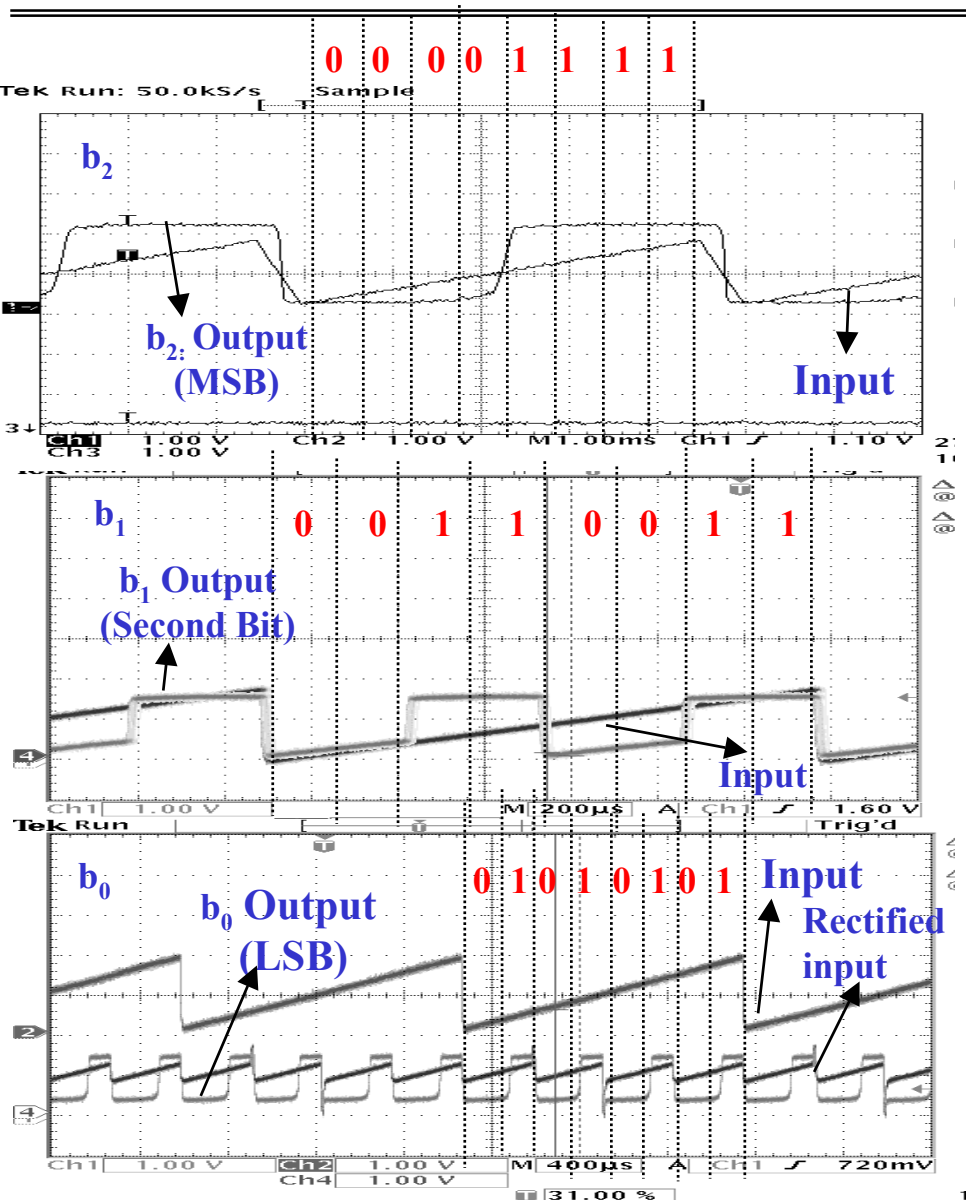
Evolution of Analog-to-Digital (ADCs)

- **ADC evolution proved harder than DAC:**
  - Multiple outputs;
  - LSB: evolution of a DC transfer with multiple peaks.
- **Approaches:**
  - Pre-process analog input (Rectification):
    - Will enable evolution of larger ADCs;
    - FPTA2 can synthesize half and full-wave rectifiers;



➢Exciting circuit with signal (C) facilitates task of evolution

3-bit ADC (b_2 b_1 b_0)



- Reconfigurable Cells:
  - 4 FPTA cells: 0,1,2,3
  - Input: 1 Analog Input (0 to 1 Volt – 10 kHz)
- Evolution Mechanism:
  - Pre-processing: rectification
  - Fitness Function: Absolute error to the target
- Genetic Algorithms
  - 400 individuals
  - Chromosome: 500 bits
  - Less than 100 generations (5 min)

Evolvable Adaptive Filter

- Demonstrate that FPTA2 can synthesize low and high pass filters without external capacitors: same piece of hardware can be reconfigured to realize low-pass and high-pass frequency responses

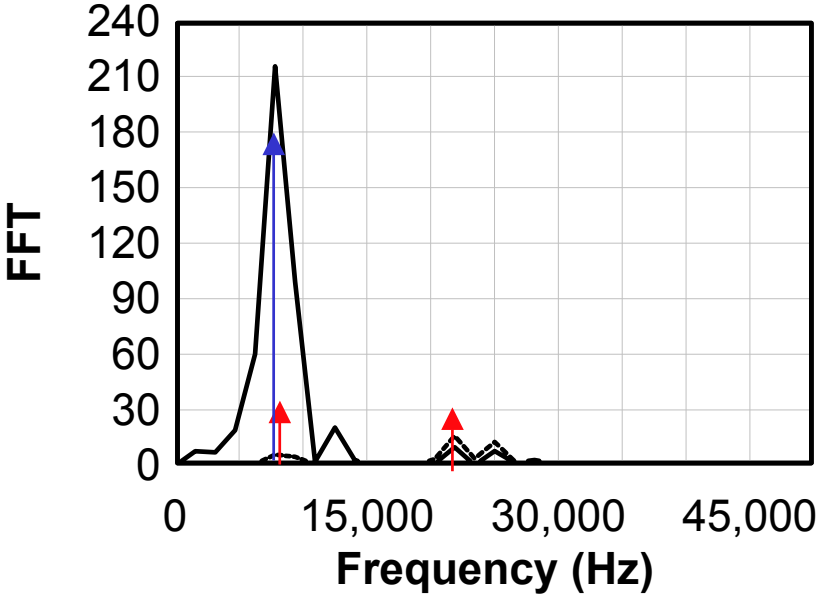
- Evolution of adaptive functionality: Filter reacts to change in the input signal
  - Evolution of filters that amplify strongest input signal and attenuate weakest signal;
  - Circuit 'does not know' frequency spectrum at the input;
  - Adaptation through reconfiguration: new circuit evolved to cope with changes at the input signal.

Low-Pass Filter

- Input signal:
  - Sum of two signals: 10kHz and 25kHz tones (10kHz has a higher amplitude);
- FPTA cells:
  - Four cells constrained to be inverters;
  - Explore resistance of switches: partly opened/closed switches;
  - Evolution of connections among cells and resistance values of switches
- Fitness Function:
  - Evaluate the FFT of output
  - Maximize output signal between 4.7kHz and 15.6kHz
- Genetic Algorithm:
  - 400 individuals/200 generations;
  - Time on SABLES: 5 min

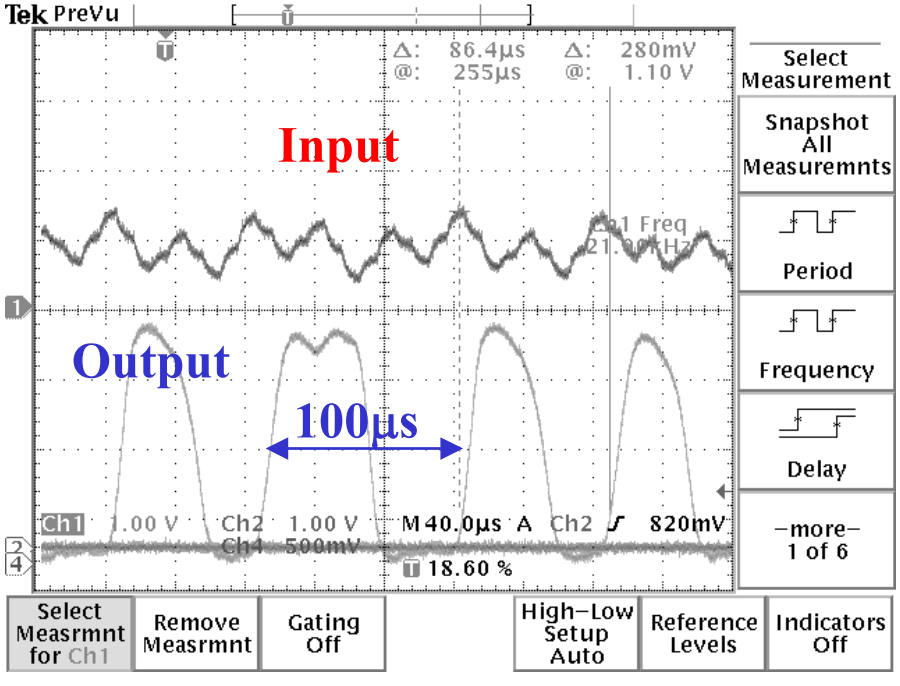
Low-Pass Filter Results

Response in the frequency domain



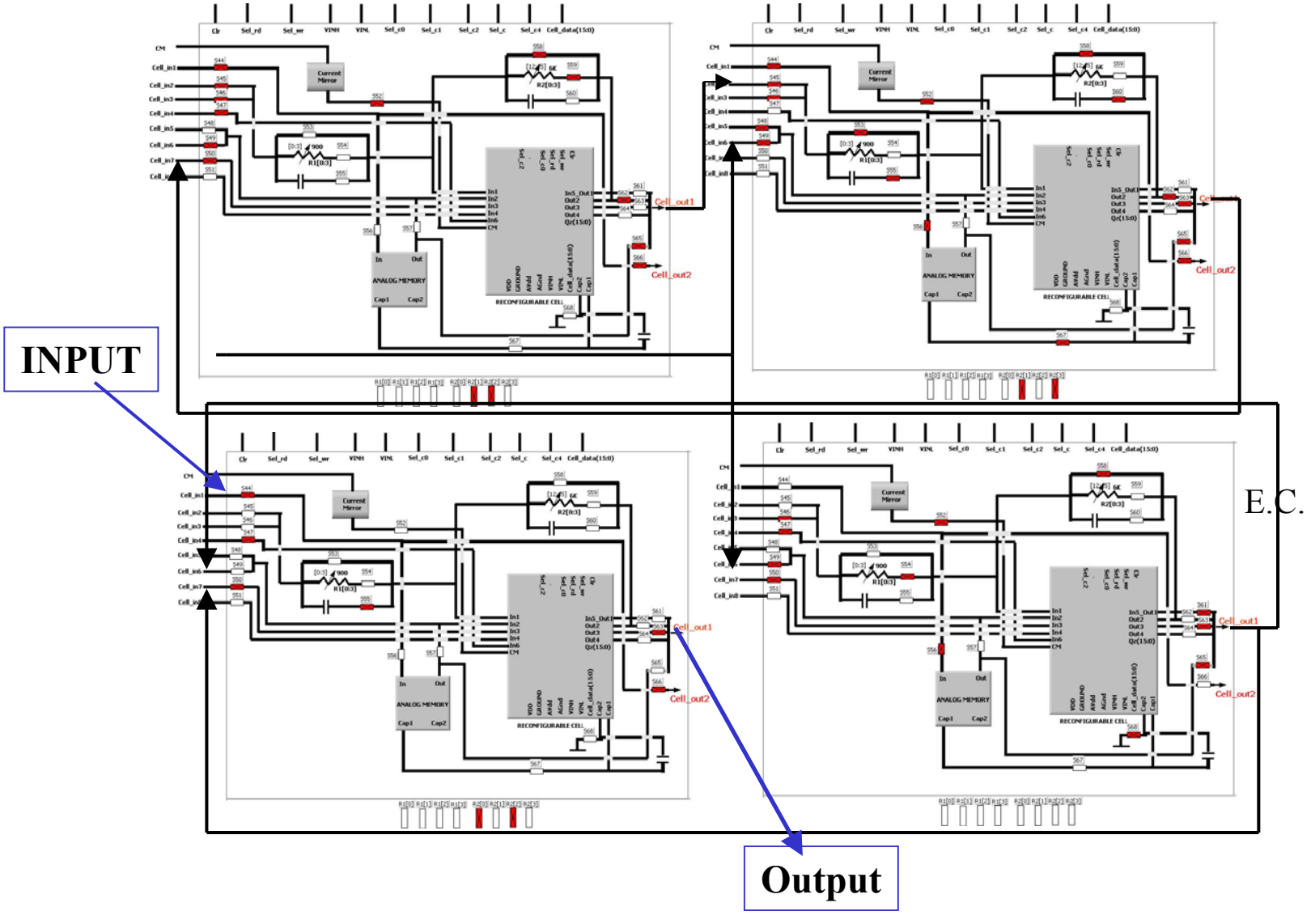
- Input: traces
- Output: full lines

Response in the time domain



- Input: scale 1V/div
- Output: scale 0.5V/div
- Time Scale: 40 µs/div
- Filter Characteristic:
  - 15.6 dB at 10kHz
  - -2.1 dB at 25 kHz

Low-Pass Filter: Evolved Circuit Schematic

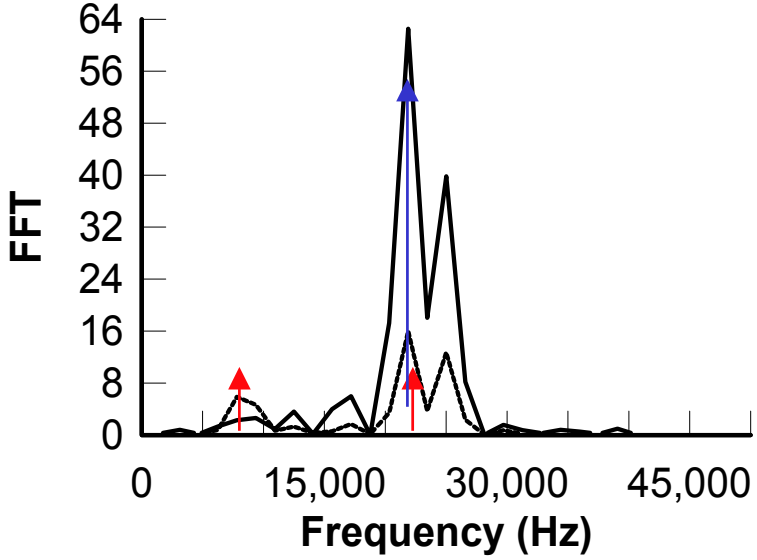


High-Pass Filter

- Input signal:
  - Sum of two signals: 10kHz and 25kHz tones (25kHz has a higher amplitude);
- FPTA cells:
  - Four cells constrained to be inverters;
  - Explore resistance of switches: partly opened/closed switches;
  - Evolution of connections among cells and resistance values of switches
- Fitness Function:
  - Evaluate the FFT of output
  - Maximize output signal between 15.6kHz and 31kHz
- Genetic Algorithm:
  - 400 individuals/200 generations;
  - Time on SABLES: 5 min

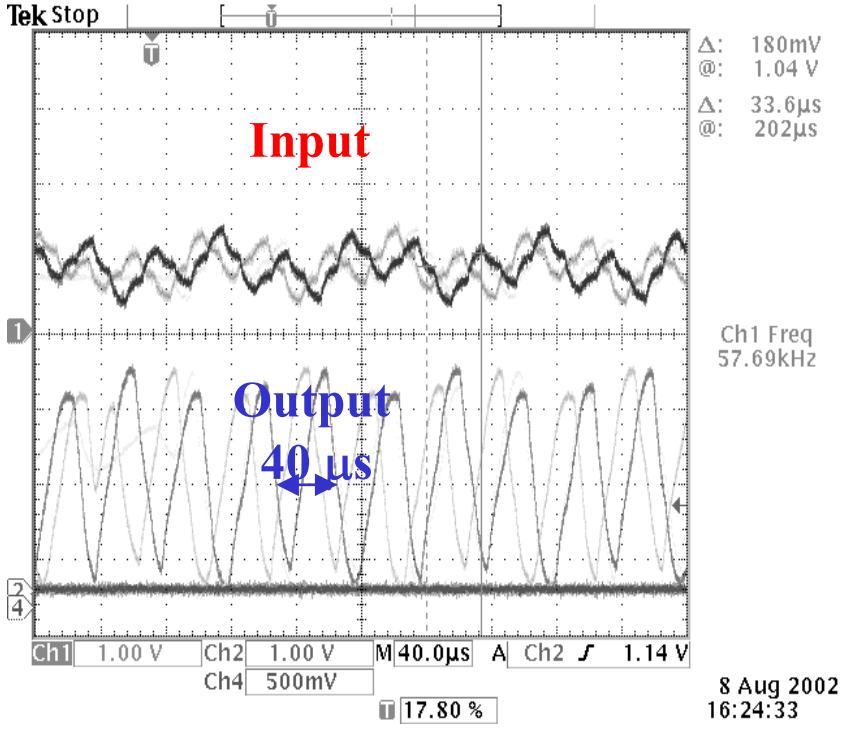
High-Pass Filter Results

Response in the frequency domain



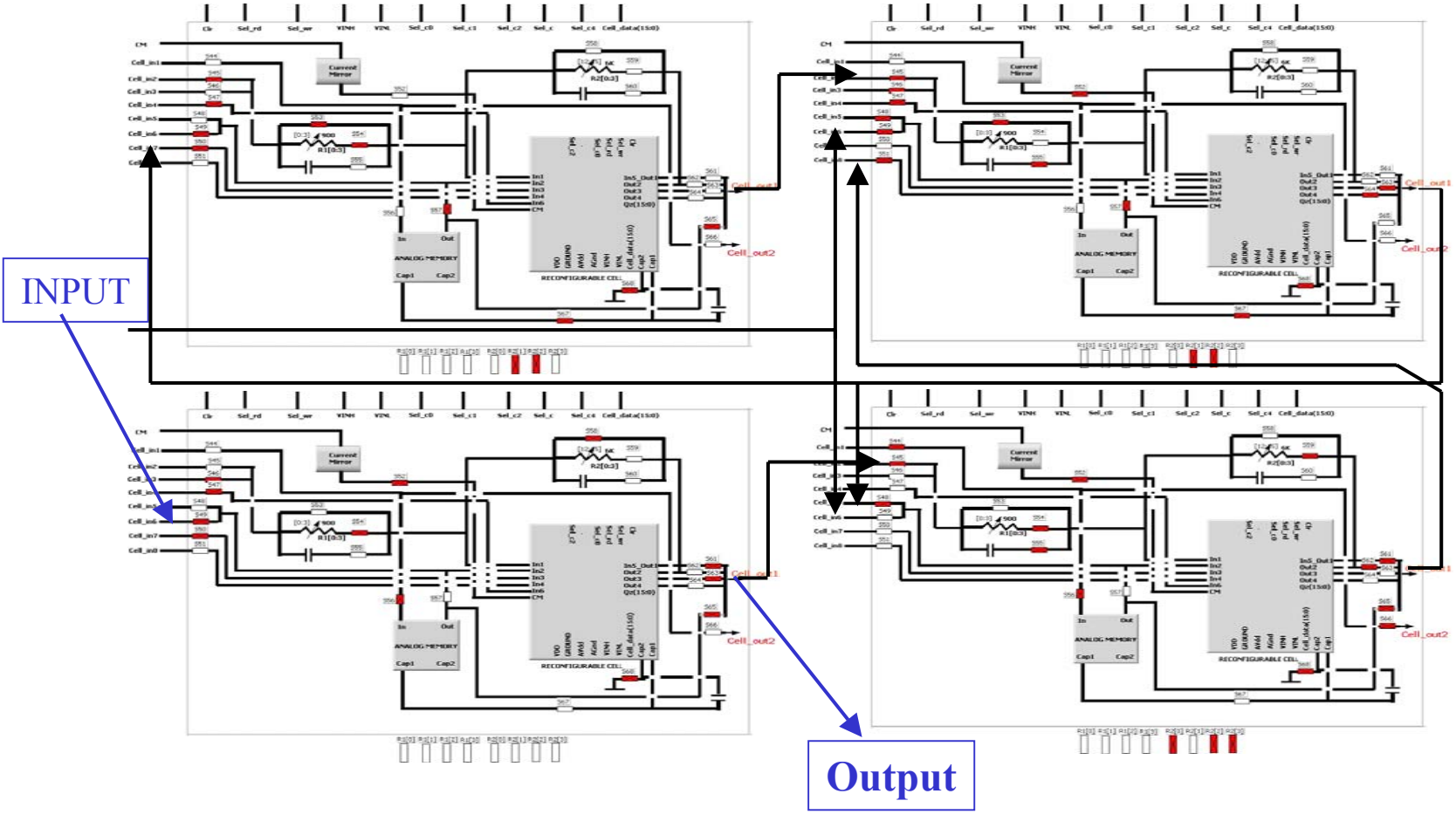
- Input: traces
- Output: full lines

Response in the time domain



- Input: scale 1V/div
- Output: scale 0.5V/div
- Time: 40 µs/div
- Filter:
  - -3.5 dB at 10 kHz
  - 5.9 dB at 25 kHz

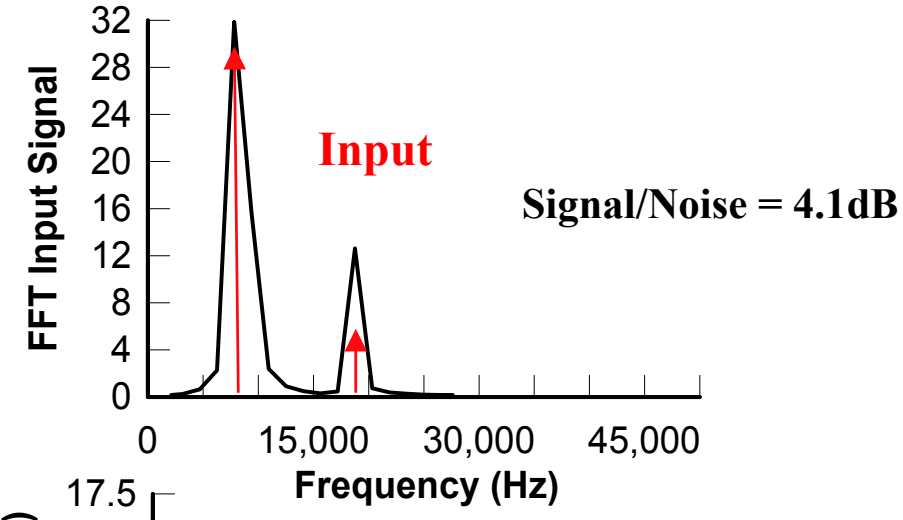
High-Pass Filter: Evolved Circuit Schematic

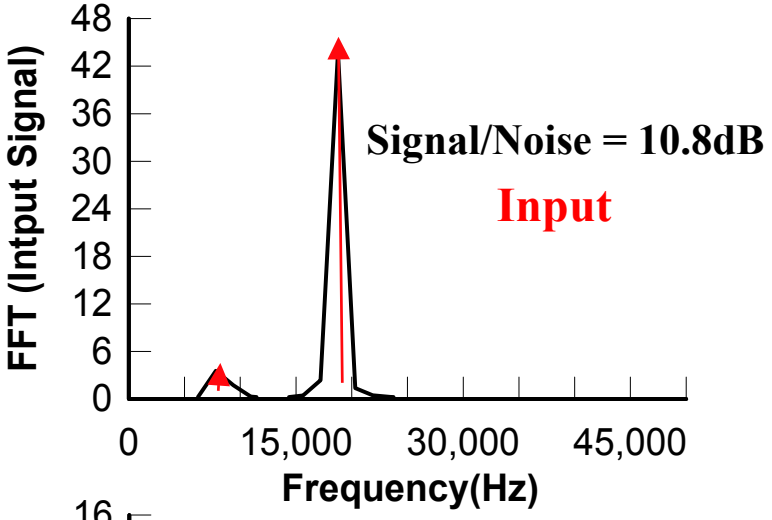


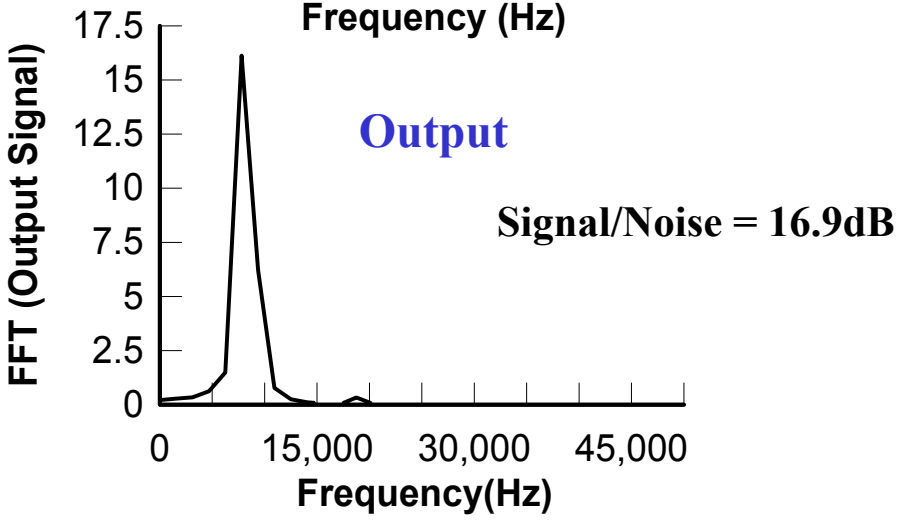
Tunable Filter

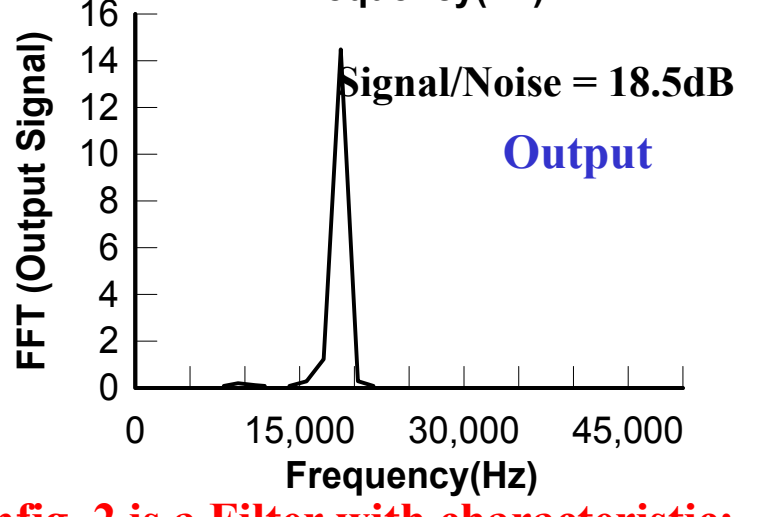
- Goal: improve signal/noise ratio
- Input signal:
  - Sum of two signals: 10kHz and 25kHz tones
  - Strong (signal) and Weak (noise) tones *not known* a priori
- FPTA cells:
  - Explore resistance of switches: partly opened/closed switches;
  - Four cells constrained to be inverters;
  - Evolved connections among cells
- Fitness Function:
  - Evaluate the FFT of output
  - Amplify strong signal, attenuate weak signal
- Genetic Algorithm:
  - 400 individuals/200 generations;
  - Time on SABLES: 5 min

Tunable Filter Results







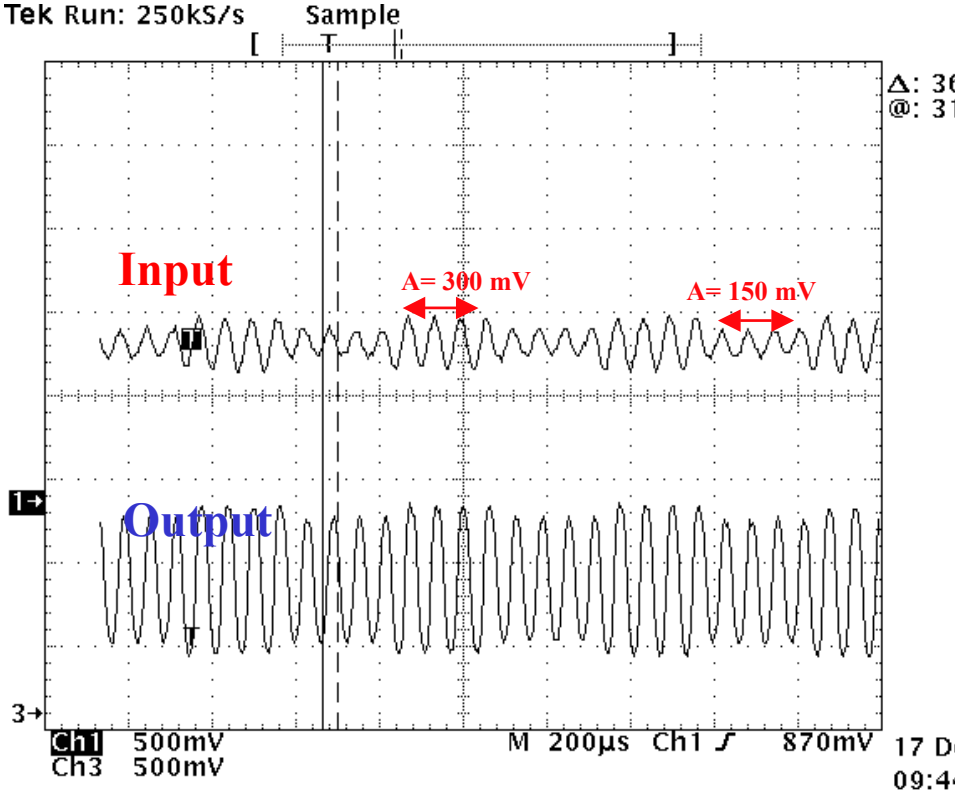


Config. 1 is a Filter with characteristic:
- **10kHz : -2.86dB attenuation**
- **20kHz : -15.8dB attenuation**

Config. 2 is a Filter with characteristic:
- **10kHz : -12.5dB attenuation**
- **20kHz : -4.8dB attenuation**

Automatic Gain Control

- Goal: Gain of the evolved circuit adapts to the amplitude of the input signal
- Fitness Function: Two input signals provided during evolution with different amplitude (150mV and 300mV). Keep the output with constant Amplitude
- 6 FPTA cells
- Results:
  - –IN = 150mV amplitude ⇒ Gain = 7
  - –IN = 300mV amplitude ⇒ Gain = 2.6
- Comments:
  - Amplifier does not saturate for 300mV input signal, e.g., the evolved behavior is not due to saturation;
  - Gain control for input signals between 150mV to 300 mV;



Graphical Interface (NIECE)

Novel Interface for an Evolutionary Computing Environment (NIECE)

Goals

- Provide a customizable data acquisition protocol to selectively collect data
- View evolution online and offline
- Save data in a compressed format
- Interface with any evolutionary system

Features

- Fully graphical user interface
- Ability to control all evolutionary parameters
- Java/C Hybrid – fully portable, optimized for speed
- Compressed storage of an entire evolutionary experiment offline
- Scrip Mode functionality
- Several Data Views
- Compatible with any evolutionary systems
- USB Interface with SABLE

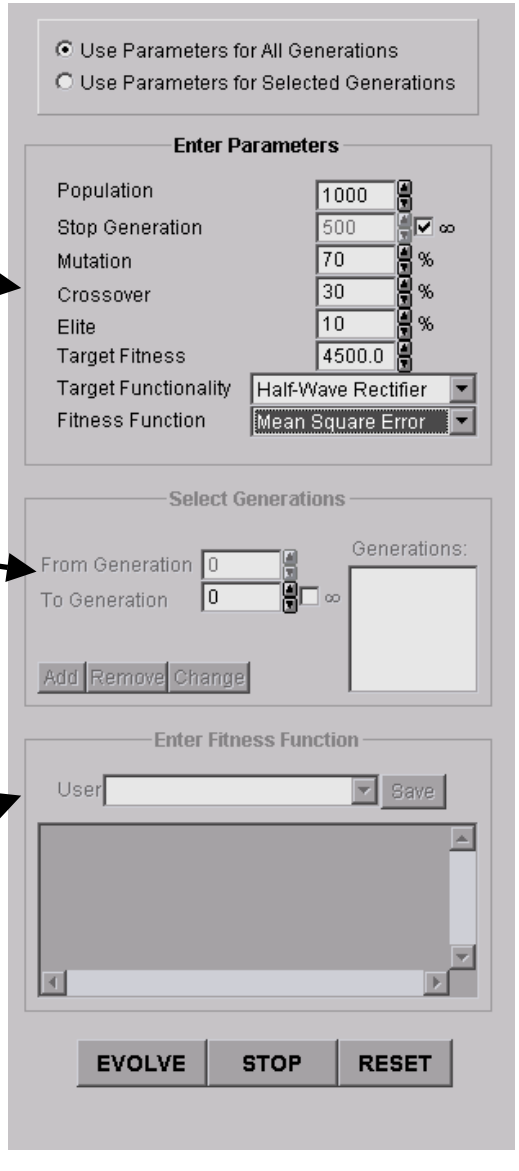
Graphical Interface - Evolutionary Controls

GA Parameters

Specify All GA Parameters at runtime

Parameters can be different per generation and changed on the fly

User specified fitness function for compilation



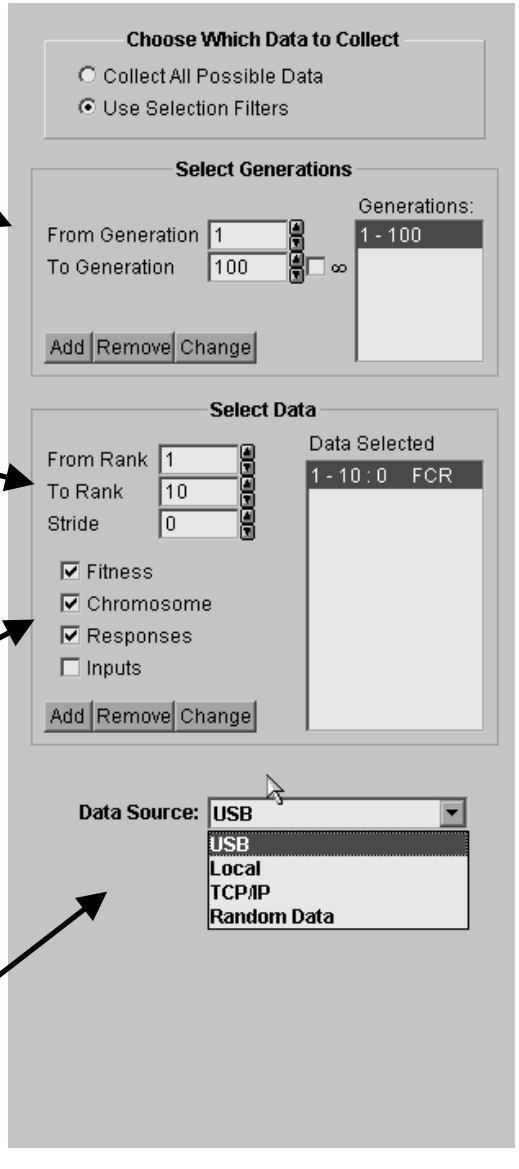
Data Acquisition

Collect data only from user specified generations

Collect only user specified individuals (from and to specified ranks, with a stride)

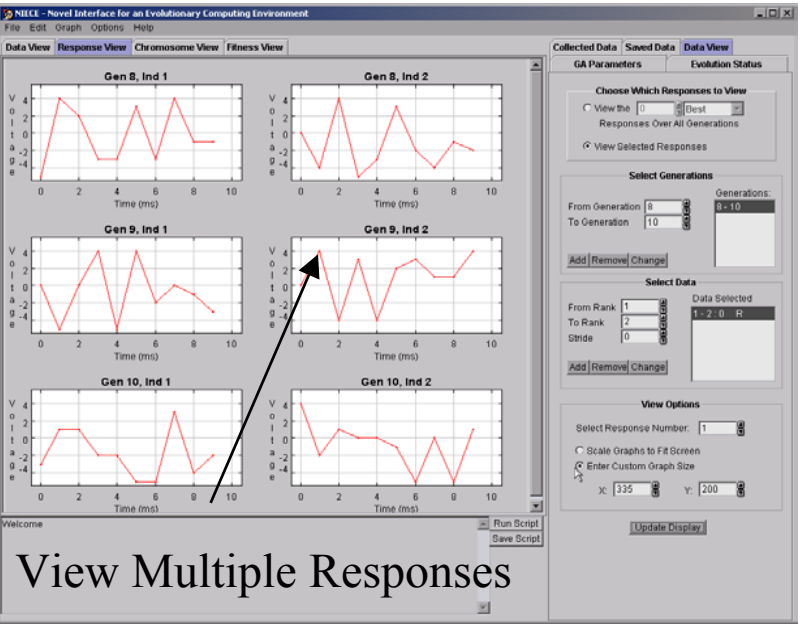
Collect only user specified data vectors

Several possible acquisition protocols



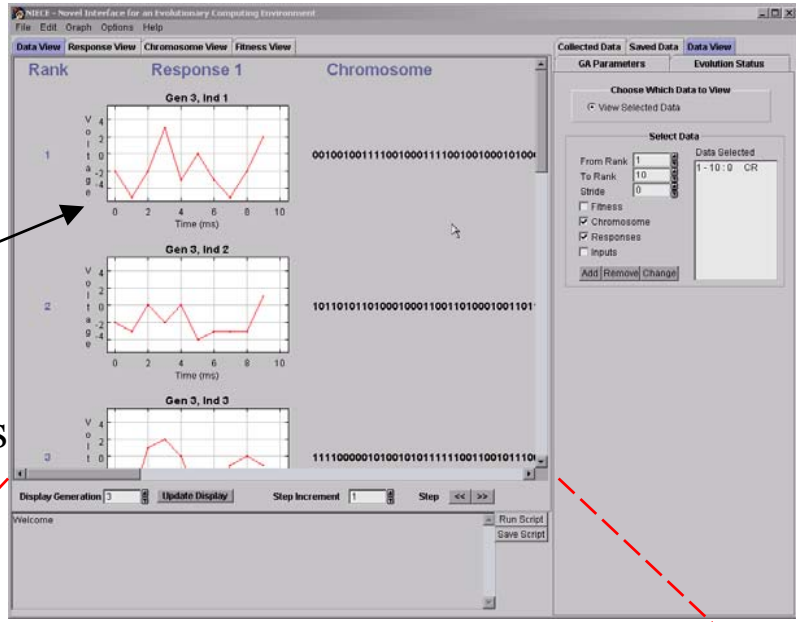
View Evolution Experiments Offline

Response View over several generations



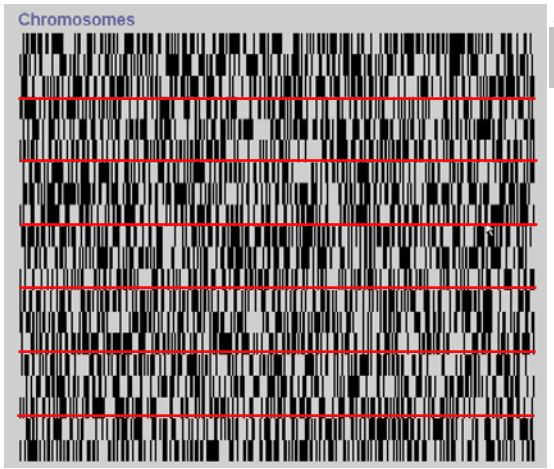
View Multiple Responses

Response view per generation



Compare Selected Individuals

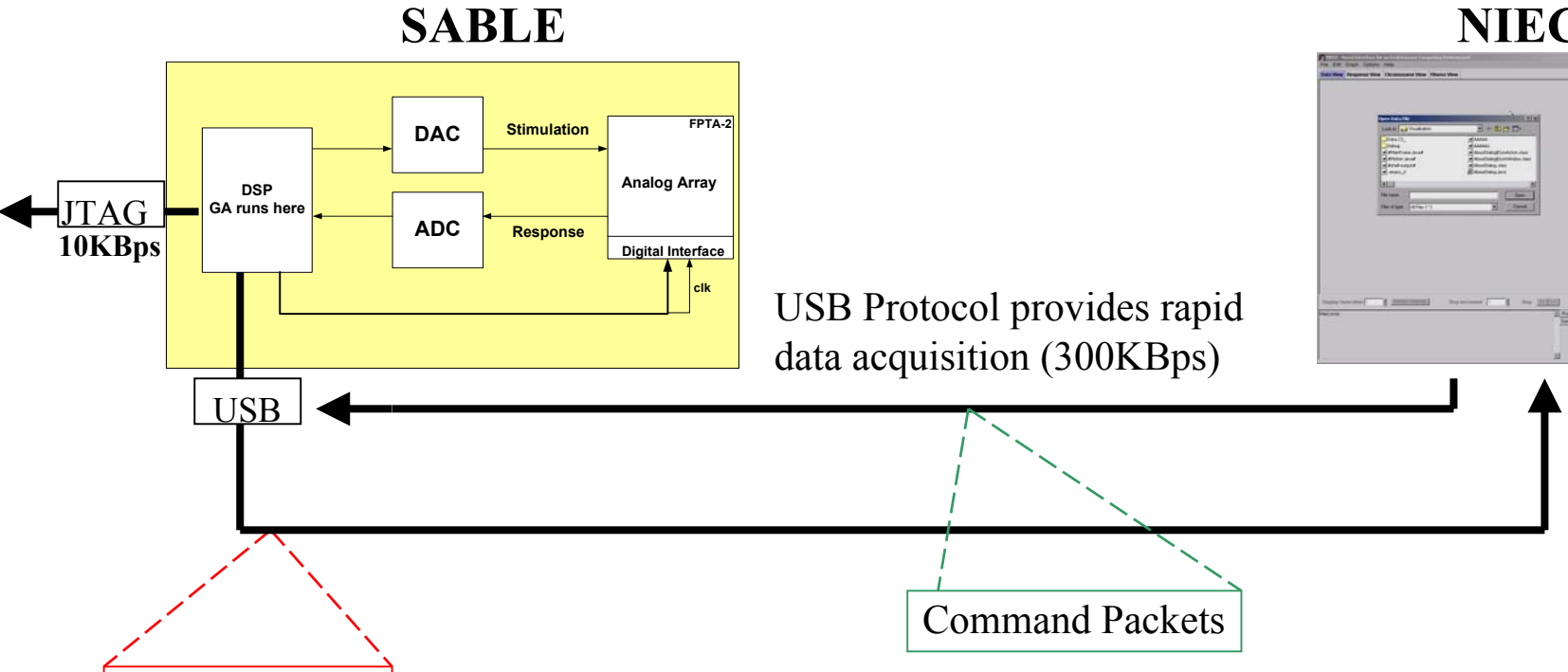
Chromosome View



Step through a previously completed evolution to recreate the experiment

Easily compare chromosomes for similarities and patterns through population and generations (3 best indiv. over 6 generations

View Evolution Experiments from/to SABLE



- Send back compressed data
- 64byte packets

Configuration bits	Fitness values	Chromosomes	Responses	Other Data

64 bytes

- Transmit all GA parameters (mutation, crossover, etc)
- 32byte packets
- Communicate customized acquisition settings – significantly reduces debugging and analysis time
- Change & control evolution on the fly

Configuration bits	GA Parameters	Acquisition Parameters

32 bytes

Planned Experiments and Research classification

- FY'03: On evolution for survivability in radiation and extreme temperature environments
  - **Experiments: submit the FPTA-2 chip to high temperature and radiation**
  - **TRL level: 2**
  - **Risk:** Medium (preliminary experiments were done with FPTA-0)
- FY'04: On development of a new evolution diehard architecture, which will seamlessly integrate the reconfigurable area, the sensing area and the evolution mechanisms
  - **Experiments: Demonstrate and Apply the diehard architecture to adaptive sensing such as StarTracker and Bio-detector (E-tongue) sensing devices**
  - **TRL level: 1**
  - **Risk:** High (the integration of sensors, reconfiguration and computation on a single die is a technological challenge)

Future Efforts / Challenges

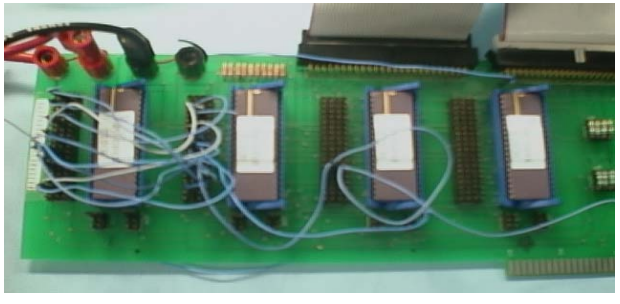
- Plan for future efforts: Evolvable hardware technology will lead to
  - ***Evolvable Hardware System on the chip***: IP core for evolvable embedded systems
  - *Integration of Evolvable Hardware with "smart Micro/Nano-scale systems":* smart skins (avionics/airplanes that heal their "wounds"), smart walls (optimize comfort with minimal energy consumption), smart implants (seeing beyond human capability)
  - *Development of tools for hybrid systems*: translating from high level specifications to morphable and evolvable device.
- Risk / Challenges:
  - The field lacks a strong formal/theoretical basis, and most work is rather empirical/experimental.
  - In most situations there is no (theoretical) way to know if a satisfactory/optimal solution exists
  - There is no guarantee that Evolvable Hardware will find a solution, even if a solution exists
  - There are no proofs of good scalability & techniques for scalability
  - Evolving hardware may be risky if intermediary (unsatisfactory solutions) can negatively impact system operation

EHW technology has the potential to be the underlying technology behind tomorrow's infrastructure, not only for electronics but also for smart optical, structural, thermal systems through reconfigurable, morphing, adaptive MEMS and materials.

APPENDIX A:
PTA Applications

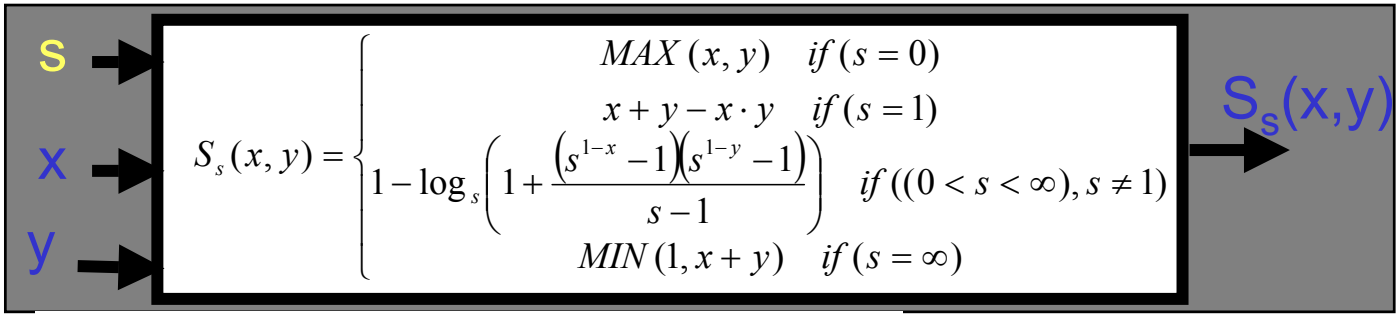
Evolved Circuits on FPTA0

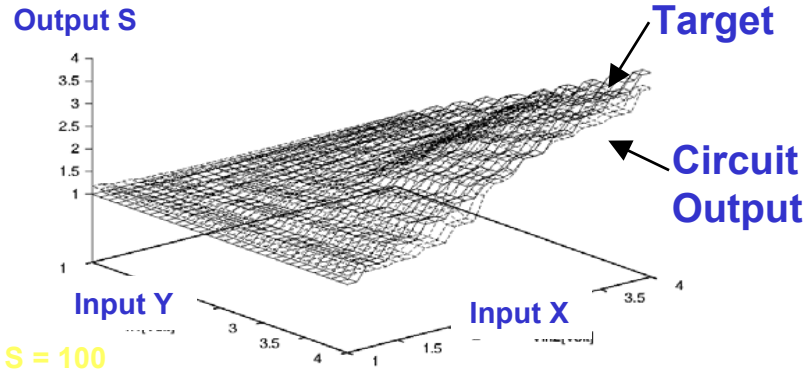
- Computational circuits: gaussian, fuzzy neurons
- multiplier
- logic circuits
- ...



Evolution of Computational circuits

Evolution of Fuzzy-Neuron Circuit





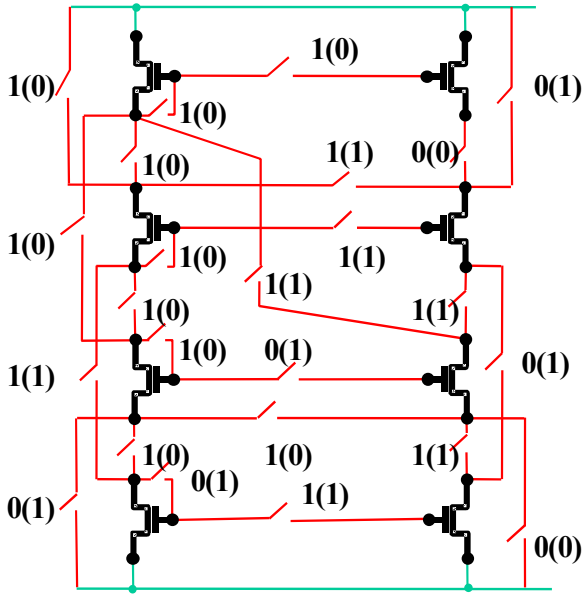
- Uses two FPTA cells (16 transistors)
- compact implementation

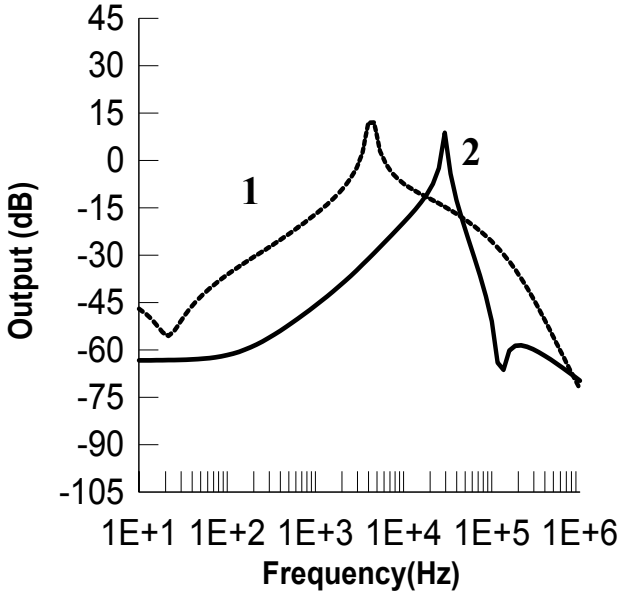
Stoica, A., In *Proceedings of the 30th IEEE Symposium on multi-valued logic*, Portland. May 2000.

Reconfigurable Filter on PTA

- Goal: demonstrate that can the PTA can synthesize band-pas filter by changing the PTA configuration.
- PTA cell:
  - Used simulation of 1 PTA cell with Spice
- Fitness Function:
  - Error to target frequency response at 5 KHz and a target frequency response at 25 kHz
- Genetic Algorithm:
  - 128 individuals/200 generations;
  - 10 min.
  - Supercomputer (128 nodes machine)

Adaptive Filter Results





Filter Characteristic:

- Configuration 1:

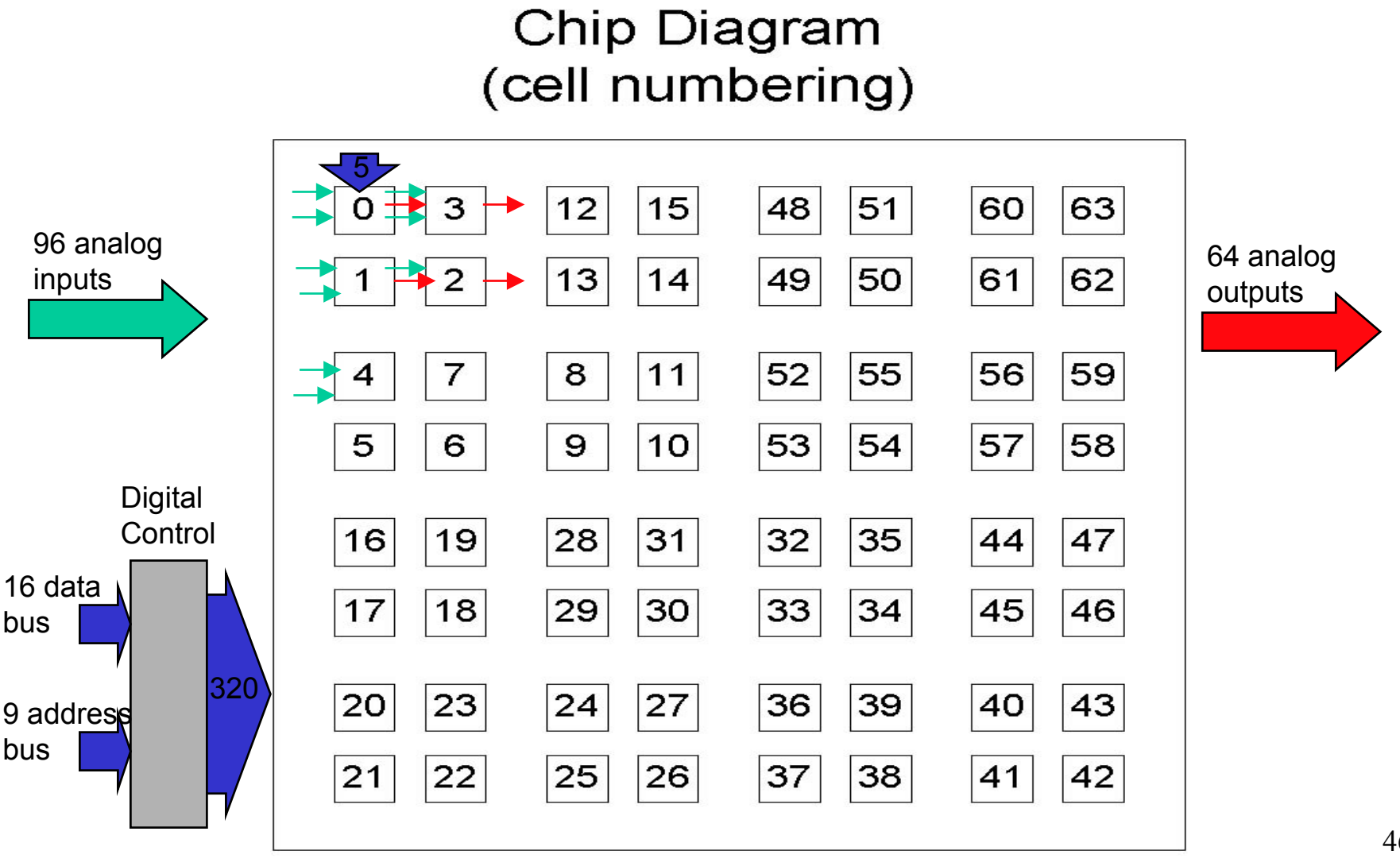
  Filter with 11dB gain at 5kHz , roll-off about –30dB/dec.

- Configuration 2 :

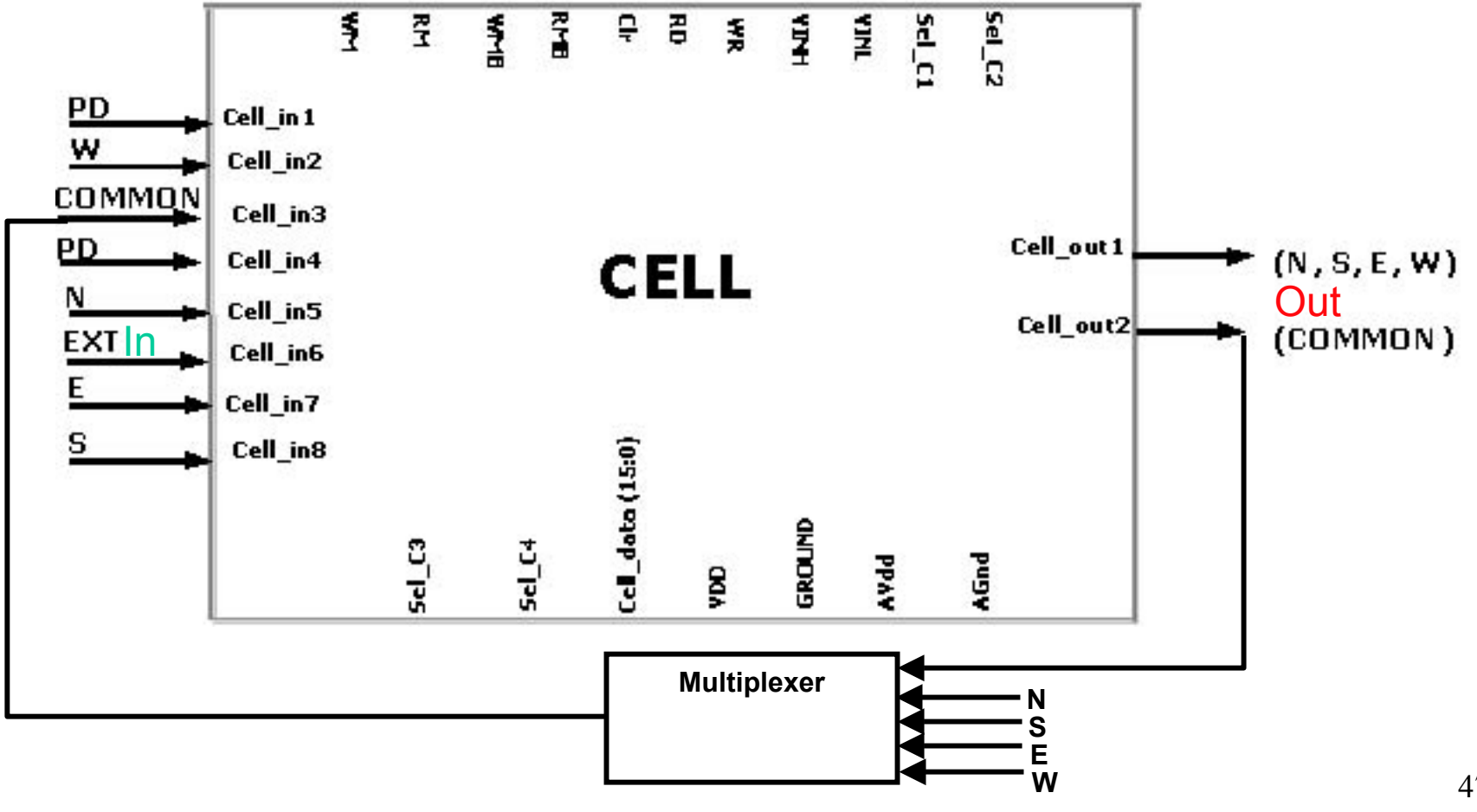
  Filter with 9dB gain at 25kHz, roll-off about –40dB/dec .

APPENDIX B:
Chip Architecture

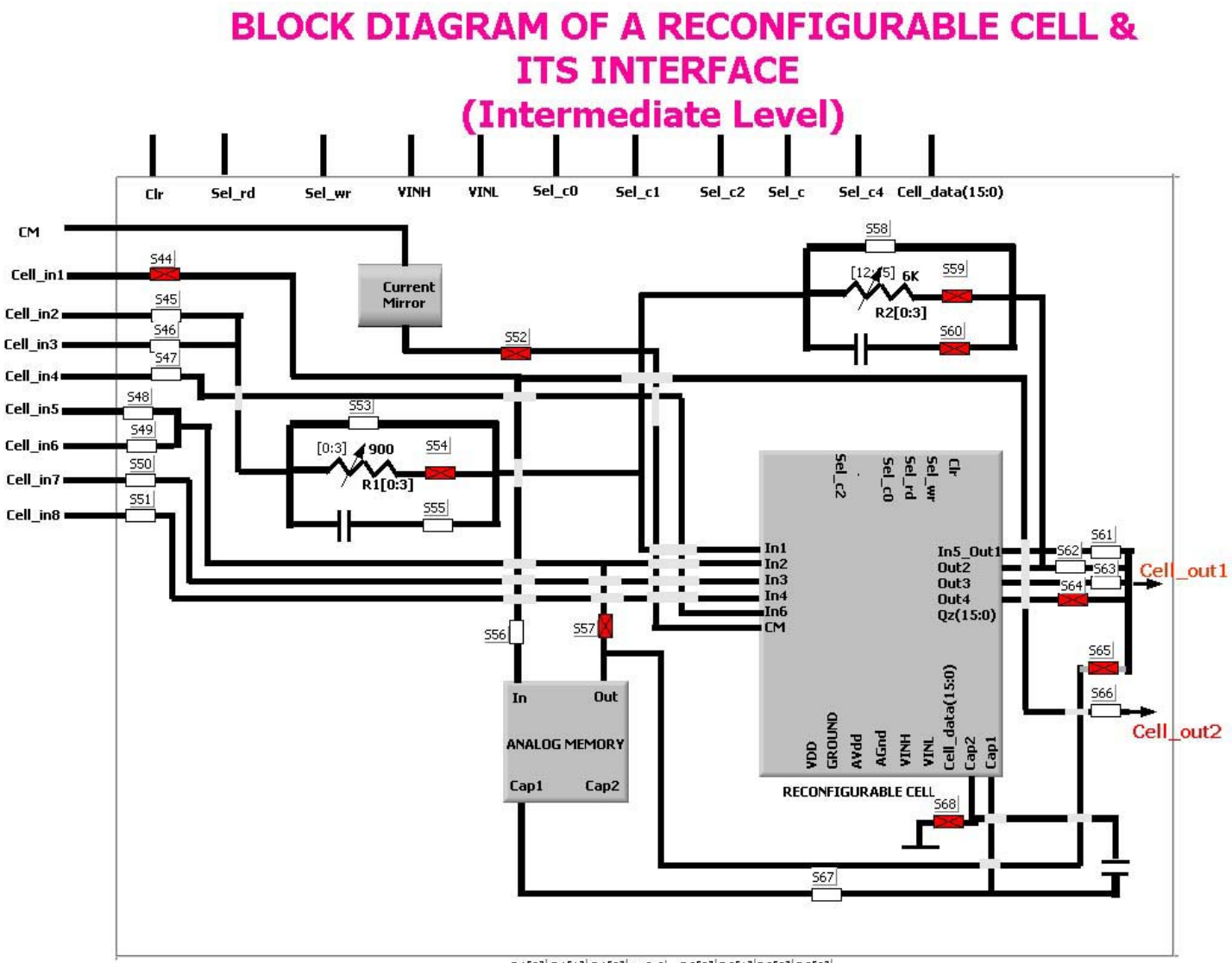
Chip Diagram



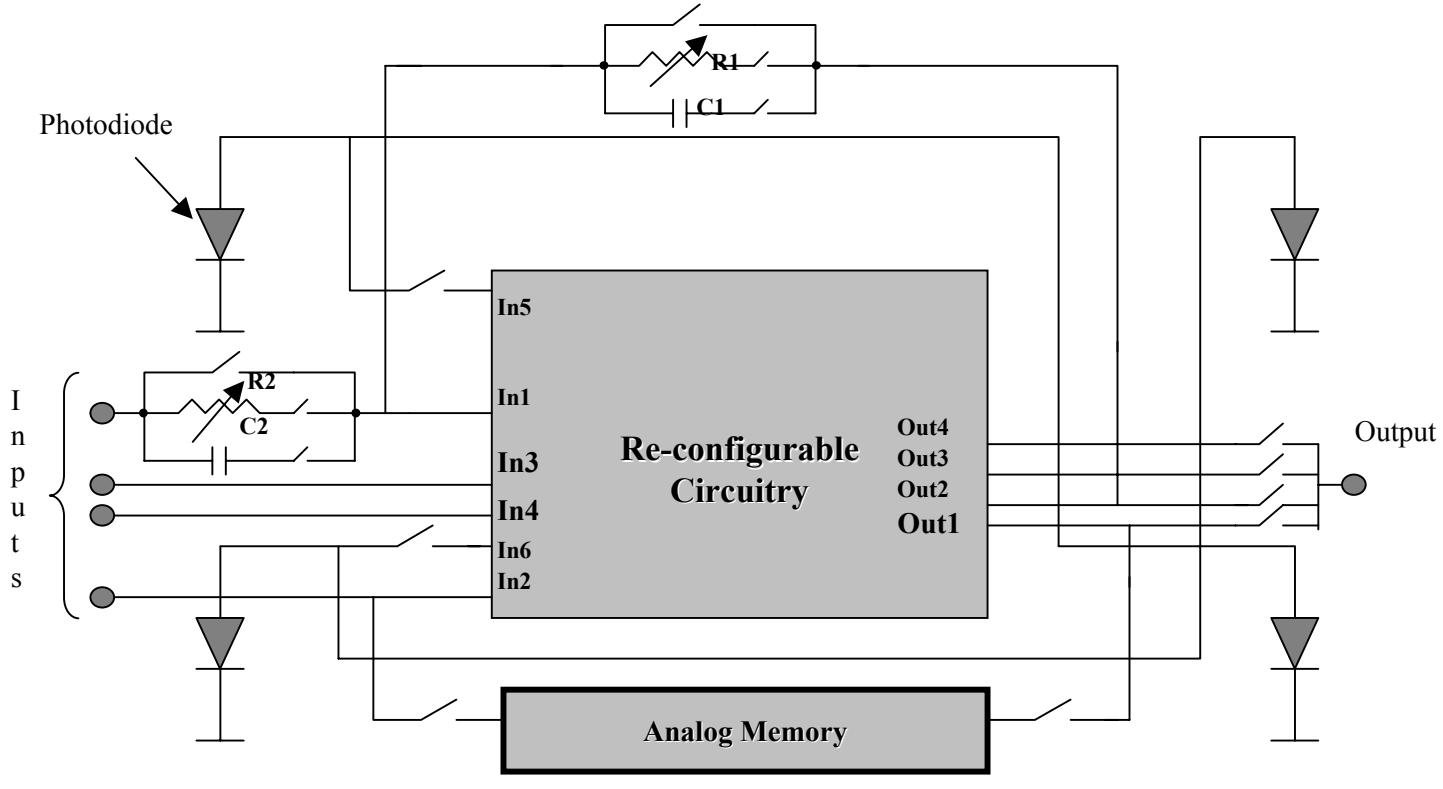
Reconfigurable Cell (Top Level)



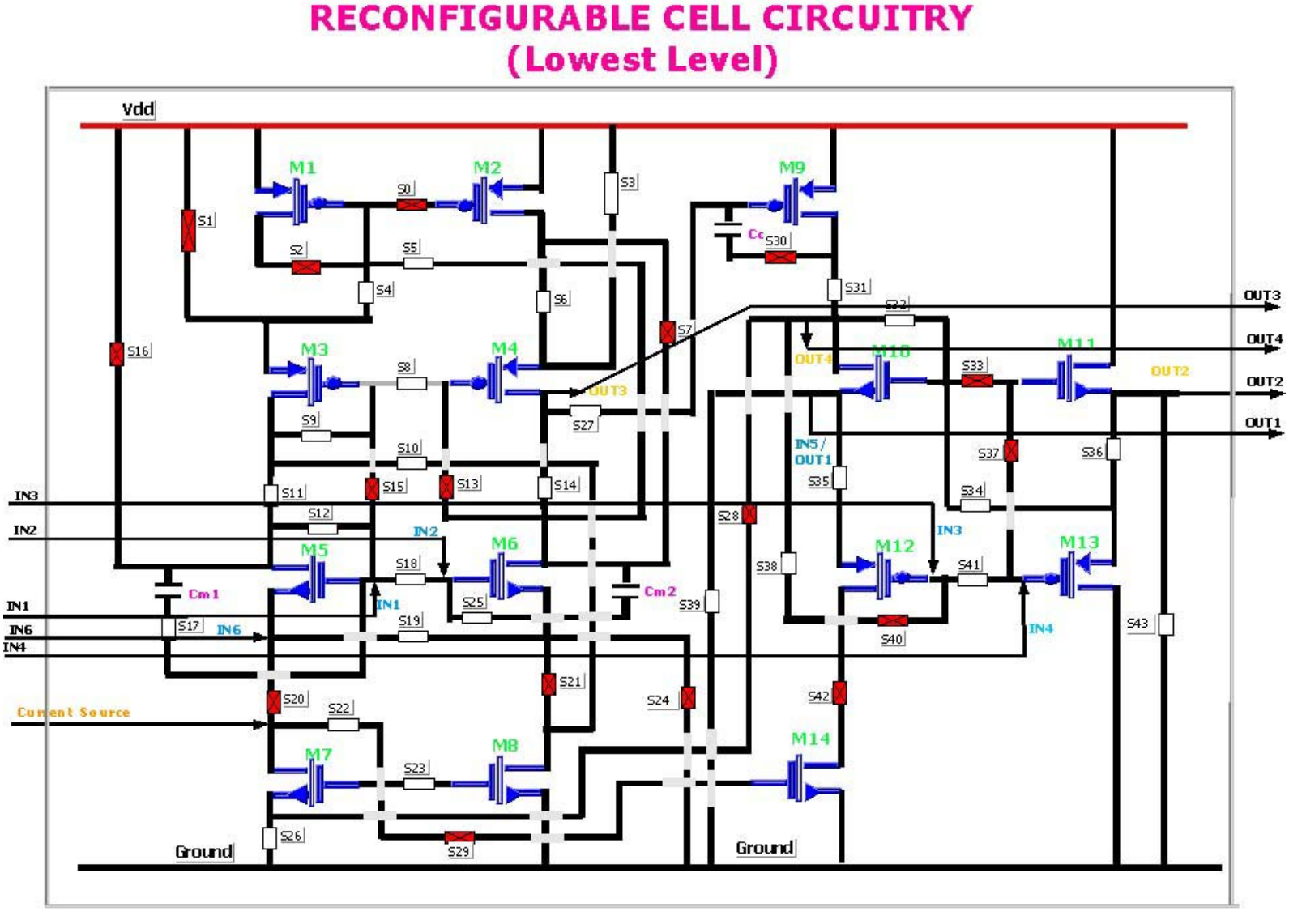
Block Diagram of Reconfigurable Cell & Interface



Block Diagram of Reconfigurable Cell & Interface

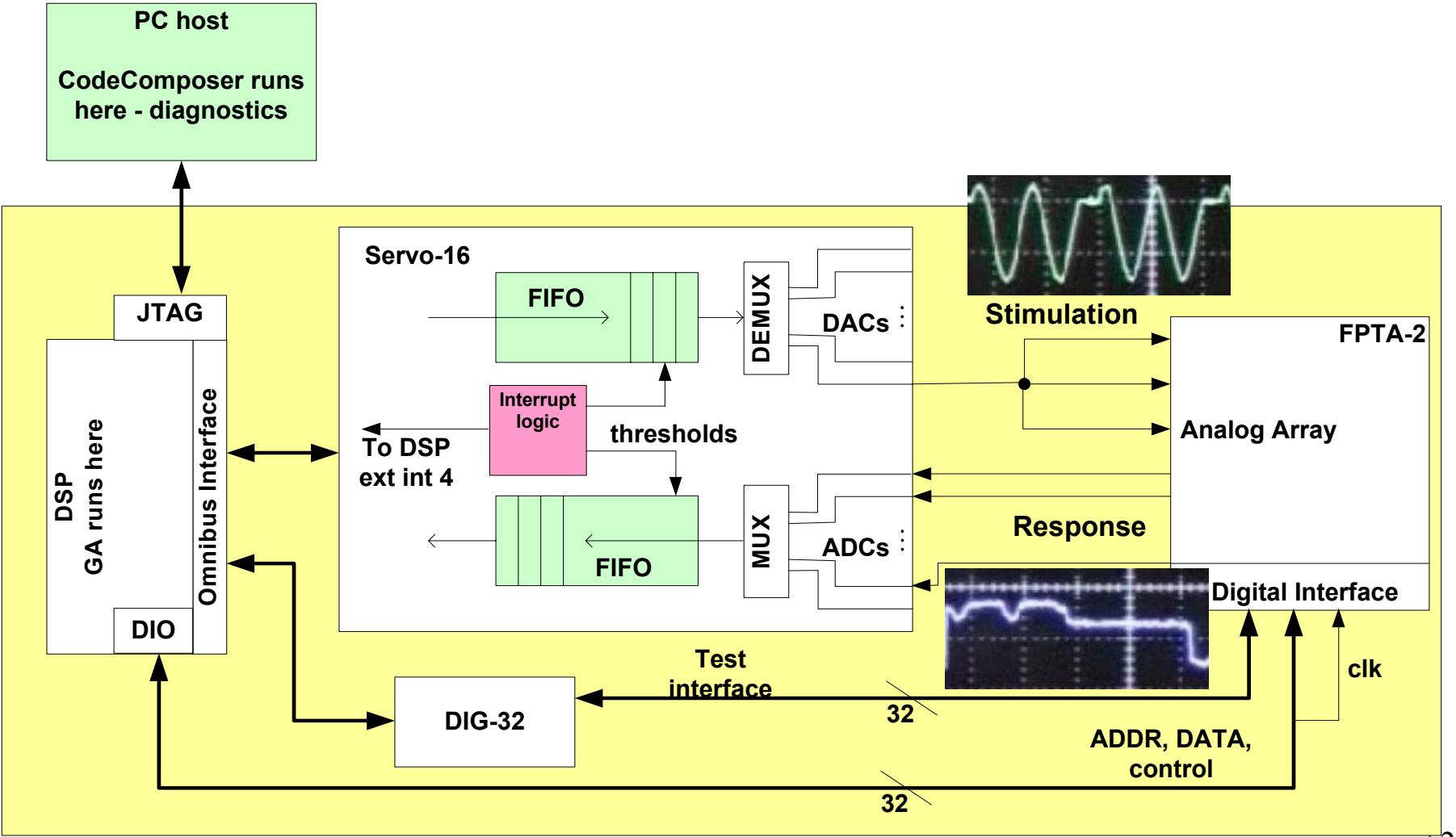


Reconfigurable Cell Circuitry (Lowest Level)



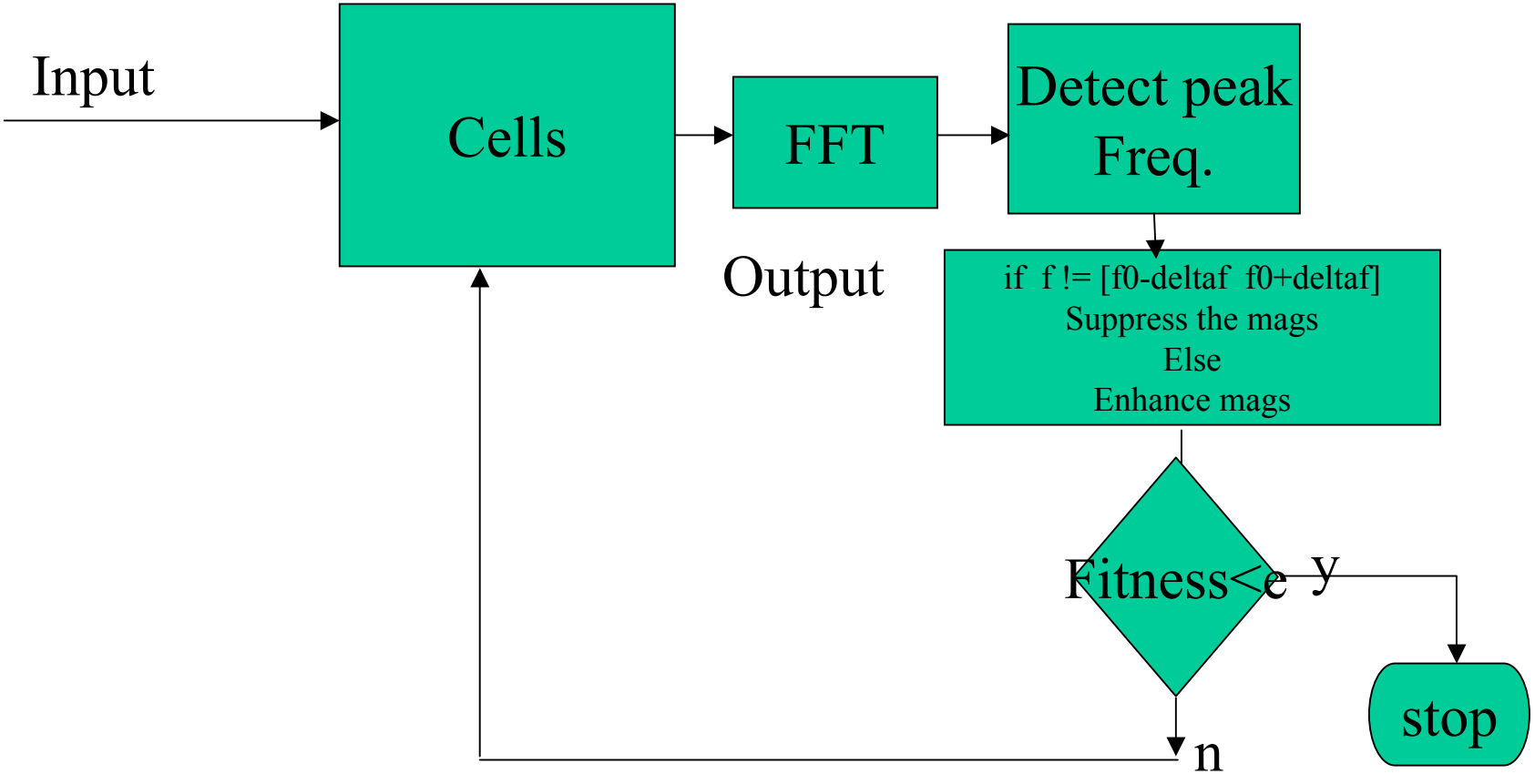
APPENDIX C:
SABLE details

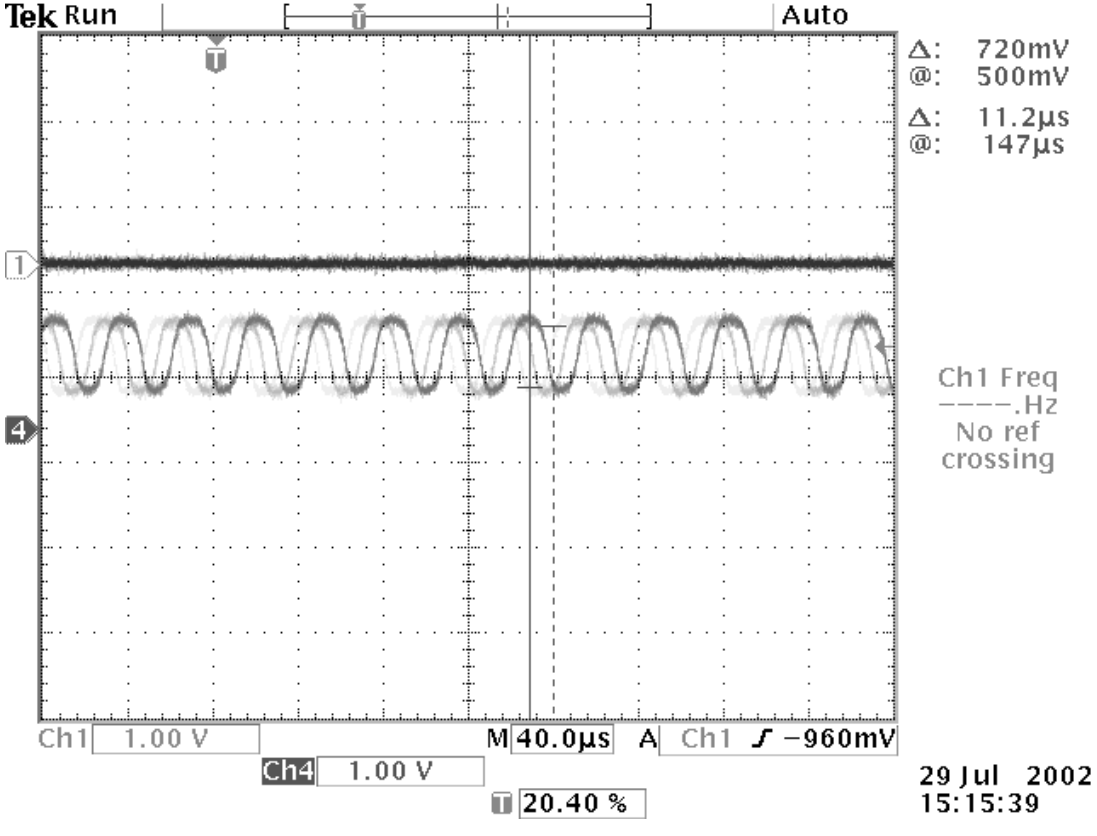
SABLE Architecture (NOT shown)



APPENDIX D:
FPTA – SABLE
Evolvable Sensing Applications

Evolvable Tunable Filter Architecture



Evolution of Oscillator

- ✓ 25kHz oscillator evolved in less than 1 minute using 4 FPTA cells with no input signals
- ✓ Chip can synthesize tones from 400Hz to 80kHz;